# CM6210

Multi-channel USB-I2S Audio Controller

## DESCRIPTION

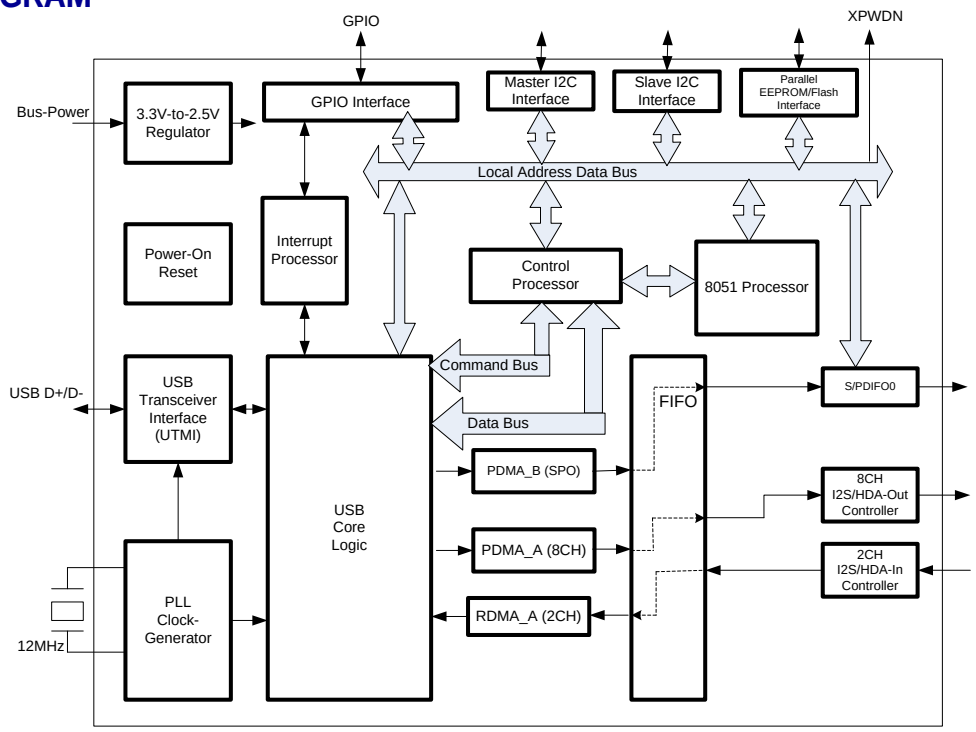
The CM6210 is a USB 2.0 full-speed/high-speed audio processor that supports the latest USB Audio Device Class V1.0. The CM6210 provides industry-standard HDA and I2S I/O interfaces, supports a maximum of 8 channels of output and 2 channels of input, and also integrates a 96KHz/24-bit S/PDIF transmitter, making it very versatile.

Furthermore, the CM6210 has an embedded 8051 microprocessor that can enhance the flexibility and functionality with external upgradeable ROM codes. The CM6210 is the most powerful audio core for your multi-channels audio products.

## FEATURES

- USB specification 2.0 full-speed/high speed-compatible
- USB audio device class 1.0-compatible
- USB human interface device (HID) class 1.1-compliant
- Supports USB suspend/resume/reset functions
- Supports control/interrupt/bulk/isochronous data transfers
- Four pairs of I2S or left-justified serial audio output interfaces (8-ch out)
- one pairs of I2S or left-justified serial audio input interfaces (2-ch in)
- I2S input/output support ( 44.1K/48KHz and 16 bits, Up to 96K/24bits for stereo )
- SPDIF output supports up to 96KHz/24-bit transfer rate

## BLOCK DIAGRAM



## Release Notes

| Revision | Date | Description |
|---|---|---|
| 0.9 | 2013/08/14 | Preliminary release |
| 0.91 | 2013/10/03 | Remove SPI interface |
| 1.0 | 2013/11/04 | Formal release |
| 1.1 | 2014/03/24 | Typo correction |
| | | |

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# 1 Description and Overview

The CM6210 is a USB 2.0 full-speed/high-speed audio processor that supports the latest USB Audio Device Class V1.0. The CM6210 provides industry-standard HDA and I2S I/O interfaces, supports a maximum of 8 channels of output and 2 channels of input, and also integrates a 96KHz/24-bit S/PDIF transmitter, making it very versatile. Furthermore, the CM6210 has an embedded 8051 microprocessor that can enhance the flexibility and functionality with external upgradeable ROM codes. The CM6210 is the most powerful audio core for your multi-channels audio products.

# 2 Features

## USB Compliance

- USB specification 2.0 full-speed/high-speed-compatible
- Latest USB audio device class 1.0-compatible
- USB human interface device (HID) Class 1.1-compliant
- Supports USB suspend/resume/reset functions
- Asynchronous synchronization transfer to reduce clock jitter
- Supports control/interrupt/bulk/isochronous data transfers

## Audio Engine

- 2 Independent playback streams:
  - Supported sample rate: 44.1K/48K/88.2K/96KHz (88.2K/96KHz are only available at stereo mode)
  - Supported bit length: 16/24-bit (24 bit is only available at stereo mode)
  - PDMA#A supports max. 8-ch to I2S output
  - PDMA#B supports S/PDIF output
- 1 Independent capture streams:
  - Supported sample rate: 44.1K/48KHz
  - Supported bit length: 16-bit
  - RDMA#A supports 2-ch from I2S input

## Audio I/O

- Four pairs of I2S or left-justified serial audio output interfaces (8-ch out)
- one pairs of I2S or left-justified serial audio input interfaces (2-ch in)

- All the I2S input/out interfaces support master/slave mode
- Built-in 96K/88.2K/48K/44.1KHz, and 16/24-bit S/PDIF transmitter

## Integrated 8051 Micro-processor

- Embedded 8051 micro-processor handles USB command transfers
- Connects to an external parallel Flash/EEPROM memory (from at least 16 kbyte up to 64 kbyte and less than 55ns access time is required) for firmware ROM codes
- HID interrupts can be implemented via firmware codes
- Provides maximum HW configuration flexibility with a firmware code upgrade
- VID/PID/product string can be customized via firmware code programming

## Control Interface

- Master I2C control interface for external audio devices or EEPROM access
- Slave I2C control interface for external MCU communication
- 7 GPIO pins

## General

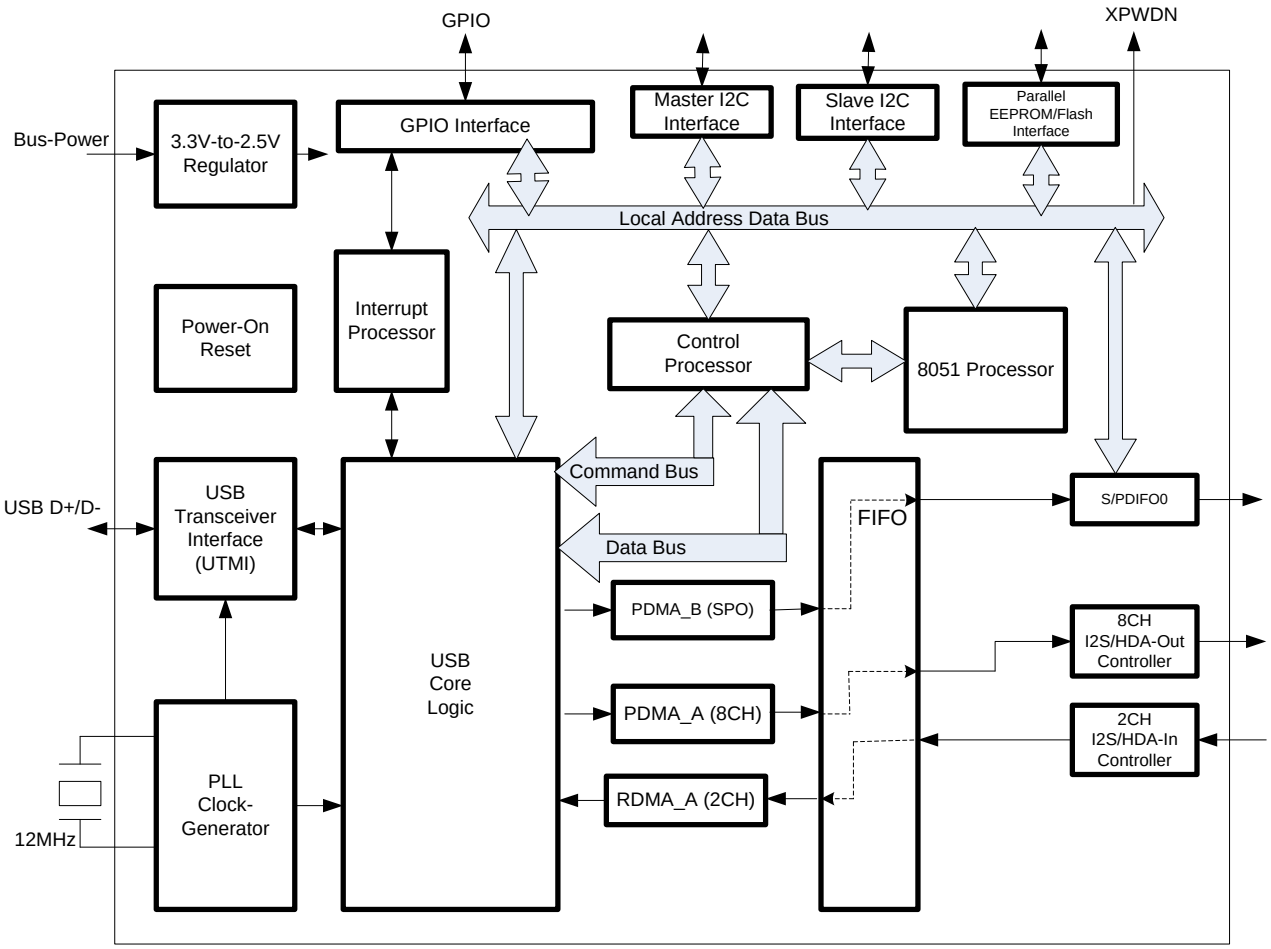
- Single 12MHz crystal input is required (for USB and embedded PLL function), and two oscillator inputs are optional (one is 49.152 or 24.576MHz for x48KHz sampling rates, and the other is 45.158 or 22.5792MHz for x44.1KHz sampling rates)
- Single 3.3V power supply (embedded 3.3V to 2.5V regulator for digital core)
- 3.3V digital I/O pads (with 5V tolerance only for GPIO and I2C pads)
- Industry-standard LQFP-80 package (10 x 10mm)

# 3 Applications

- PC gaming headset: USB 5.1/7.1 virtual surround gaming headset with embedded DSP processing (no driver installation required)
- Game console +PC combo gaming headset: supports 5.1/7.1 surround sounds on multi-platforms (wired or wireless headsets)
- High quality multi-channel sound stations (audio boxes)

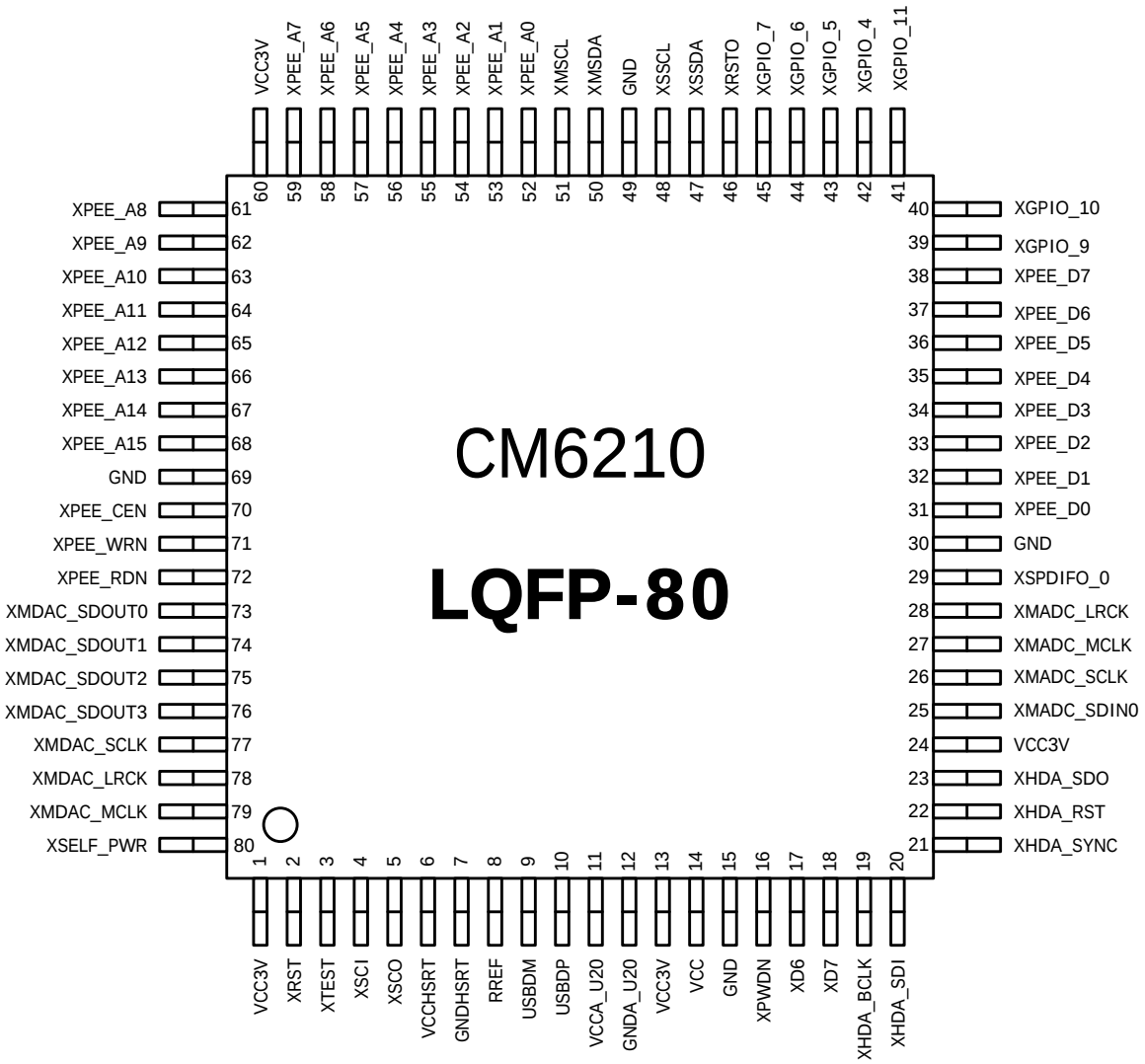
# 4 Block Diagram

**CM6210 Functional Block Diagram**



# 5 Pin Assignment

## 5.1 Pin-Out Diagram



## 5.2 Pin Description

| Pin # | Symbol | I/O | Description |
|---|---|---|---|
| **Clock** | | | |
| 5 | XSCO | AO | 12MHz crystal oscillator output |
| 4 | XSCI | AI | 12MHz crystal oscillator input |
| 17 | XD6 | DIO | 49.152/24.576MHz oscillator input(for 48, 96KHz) |
| 18 | XD7 | DIO | 45.158/22.5792MHz oscillator input(for 44.1KHz) |
| **USB 2.0 Bus Interface** | | | |
| 9 | USBDM | AIO | USB 2.0 data negative (USB D- signal) |
| 10 | USBDP | AIO | USB 2.0 data positive (USB D+ signal) |
| **Power/Ground** | | | |
| 6 | VCCHSRT | AI | USB PHY analog power supply pin (3.3V) |
| 7 | GNDHSRT | AI | USB PHY analog ground |
| 11 | VCCA_U20 | AI | USB PHY analog power supply pin (3.3V) |
| 12 | GNDA_U20 | A | USB PHY analog ground |
| 1 | VCC3V | DI | Digital power supply pin (3.3V) |
| 14 | VCC | DO | Digital power filter pin (2.5V), connecting external filter capacitors |
| 15 | GND | D | Digital ground |
| 30 | GND | D | Digital ground |
| 13 | VCC3V | DI | Digital power supply pin (3.3V) |
| 49 | GND | D | Digital ground |
| 24 | VCC3V | DI | Digital power supply pin (3.3V) |
| 69 | GND | D | Digital ground |
| 60 | VCC3V | DI | Digital power supply pin (3.3V) |
| **2-channel I2S ADC_1 Interface (RDMA_A)** | | | |
| 25 | XMADC_SDIN0 | DI | I2S serial data input for channel 0, 1<br>Programmable 3.3V input buffer, Schmitt trigger, pull-down |
| 26 | XMADC_SCLK | DIO | I2S bit clock<br>Programmable 3.3V bidirectional buffer, pull-down |
| 27 | XMADC_MCLK | DO | I2S master clock<br>Programmable 3.3V output buffer |
| 28 | XMADC_LRCK | DIO | I2S left/right clock<br>Programmable 3.3V bidirectional buffer, pull-down |
| **S/PDIF Output** | | | |
| 29 | XSPDIFO_0 | DO | S/PDIF transmitter<br>Programmable 3.3V output buffer |
| **Parallel EEPROM/Flash Memory Interface** | | | |
| 31 | XPEE_D0 | DIO | Parallel EEPROM/FLASH data in/out 0<br>Programmable 3.3V bidirectional buffer, pull-down |

| | | | |
|---|---|---|---|
| 32 | XPEE_D1 | DIO | Parallel EEPROM/FLASH data in/out 1<br>Programmable 3.3V bidirectional buffer, pull-down |
| 33 | XPEE_D2 | DIO | Parallel EEPROM/FLASH data in/out 2<br>Programmable 3.3V bidirectional buffer, pull-down |
| 34 | XPEE_D3 | DIO | Parallel EEPROM/FLASH data in/out 3<br>Programmable 3.3V bidirectional buffer, pull-down |
| 35 | XPEE_D4 | DIO | Parallel EEPROM/FLASH data in/out 4<br>Programmable 3.3V bidirectional buffer, pull-down |
| 36 | XPEE_D5 | DIO | Parallel EEPROM/FLASH data in/out 5<br>Programmable 3.3V bidirectional buffer, pull-down |
| 37 | XPEE_D6 | DIO | Parallel EEPROM/FLASH data in/out 6<br>Programmable 3.3V bidirectional buffer, pull-down |
| 38 | XPEE_D7 | DIO | Parallel EEPROM/FLASH data in/out 7<br>Programmable 3.3V bidirectional buffer, pull-down |
| 70 | XPEE_CEN | DO | Parallel EEPROM/FLASH chip enable, active low<br>Programmable 3.3V output buffer |
| 71 | XPEE_WRN | DIO | Parallel EEPROM/FLASH write enable, active low<br>Programmable 3.3V bidirectional buffer, pull-down |
| 72 | XPEE_RDN | DIO | Parallel EEPROM/FLASH read enable, active low<br>Programmable 3.3V bidirectional buffer, pull-down |
| 52 | XPEE_A0 | DIO | Parallel EEPROM/FLASH address 0<br>Programmable 3.3V bidirectional buffer, pull-down |
| 53 | XPEE_A1 | DIO | Parallel EEPROM/FLASH address 1<br>Programmable 3.3V bidirectional buffer, pull-down |
| 54 | XPEE_A2 | DIO | Parallel EEPROM/FLASH address 2<br>Programmable 3.3V bidirectional buffer, pull-down |
| 55 | XPEE_A3 | DIO | Parallel EEPROM/FLASH address 3<br>Programmable 3.3V bidirectional buffer, pull-down |
| 56 | XPEE_A4 | DIO | Parallel EEPROM/FLASH address 4<br>Programmable 3.3V bidirectional buffer, pull-down |
| 57 | XPEE_A5 | DIO | Parallel EEPROM/FLASH address 5<br>Programmable 3.3V bidirectional buffer, pull-down |
| 58 | XPEE_A6 | DIO | Parallel EEPROM/FLASH address 6<br>Programmable 3.3V bidirectional buffer, pull-down |
| 59 | XPEE_A7 | DIO | Parallel EEPROM/FLASH address 7<br>Programmable 3.3V bidirectional buffer, pull-down |
| 61 | XPEE_A8 | DIO | Parallel EEPROM/FLASH address 8<br>Programmable 3.3V bidirectional buffer, pull-down |
| 62 | XPEE_A9 | DIO | Parallel EEPROM/FLASH address 9<br>Programmable 3.3V bidirectional buffer, pull-down |
| 63 | XPEE_A10 | DIO | Parallel EEPROM/FLASH address 10<br>Programmable 3.3V bidirectional buffer, pull-down |
| 64 | XPEE_A11 | DIO | Parallel EEPROM/FLASH address 11<br>Programmable 3.3V bidirectional buffer, pull-down |
| 65 | XPEE_A12 | DIO | Parallel EEPROM/FLASH address 12<br>Programmable 3.3V bidirectional buffer, pull-down |
| 66 | XPEE_A13 | DIO | Parallel EEPROM/FLASH address 13<br>Programmable 3.3V bidirectional buffer, pull-down |
| 67 | XPEE_A14 | DIO | Parallel EEPROM/FLASH address 14<br>Programmable 3.3V bidirectional buffer, pull-down |
| 68 | XPEE_A15 | DIO | Parallel EEPROM/FLASH address 15<br>Programmable 3.3V bidirectional buffer, pull-down |
| **GPIO** | | | |
| 42 | XGPIO_4 | DIO | General purpose input/output 4 (default input).<br>Programmable 3.3V/5V tolerance bidirectional buffer, pull-down |
| 43 | XGPIO_5 | DIO | General purpose input/output 5 (default input).<br>Programmable 3.3V/5V tolerance bidirectional buffer, pull-down |
| 44 | XGPIO_6 | DIO | General purpose input/output 6 (default input).<br>Programmable 3.3V/5V tolerance bidirectional buffer, pull-down |
| 45 | XGPIO_7 | DIO | General purpose input/output 7 (default input).<br>Programmable 3.3V/5V tolerance bidirectional buffer, pull-down |
| 39 | XGPIO_9 | DIO | General purpose input/output 9 (default output).<br>Programmable 3.3V/5V tolerance bidirectional buffer, pull-down |

| | | | |
|---|---|---|---|
| 40 | XGPIO_10 | DIO | General purpose input/output 10 (default input).<br>Programmable 3.3V/5V tolerance bidirectional buffer, pull-down |
| 41 | XGPIO_11 | DIO | General purpose input/output 11 (default input).<br>Programmable 3.3V/5V tolerance bidirectional buffer, pull-down |
| **High-Definition Audio Interface** | | | |
| 19 | XHDA_BCLK | DO | HDA link bit clock (24MHz)<br>Programmable 3.3V output buffer |
| 20 | XHDA_SDI | DI | HDA link serial data in<br>Programmable 3.3V bidirectional buffer, pull-down |
| 21 | XHDA_SYNC | DO | HDA link frame synchronization<br>Programmable 3.3V output buffer |
| 22 | XHDA_RST | DO | HDA link reset signal, active low<br>Programmable 3.3V output buffer |
| 23 | XHDA_SDO | DO | HDA link serial data out<br>Programmable 3.3V output buffer |
| **8-channel I2S or 2-channel DSD DAC_1 Interface (PDMA_A)** | | | |
| 73 | XMDAC_SDOUT0 | DO | I2S serial data output for channel 0, 1/DSD left channel data<br>Programmable 3.3V output buffer |
| 74 | XMDAC_SDOUT1 | DO | I2S serial data output for channel 2, 3/DSD right channel data<br>Programmable 3.3V output buffer |
| 75 | XMDAC_SDOUT2 | DO | I2S serial data output for channel 4, 5<br>Programmable 3.3V output buffer |
| 76 | XMDAC_SDOUT3 | DO | I2S serial data output for channel 6, 7<br>Programmable 3.3V output buffer |
| 77 | XMDAC_SCLK | DIO | I2S bit clock/DSD Serial clock<br>Programmable 3.3V bidirectional buffer, pull-down |
| 78 | XMDAC_LRCK | DIO | I2S left/right clock<br>Programmable 3.3V bidirectional buffer, pull-down |
| 79 | XMDAC_MCLK | DO | I2S master clock<br>Programmable 3.3V output buffer |
| **2-Wire Master Serial Bus (I2C)** | | | |
| 50 | XMSDA | DIO | 2-wire master serial data<br>Programmable 3.3V/5V tolerant bidirectional buffer, pull-down |
| 51 | XMSCL | DIO | 2-wire master serial clock<br>Programmable 3.3V/5V tolerant bidirectional buffer, pull-down |
| **2-Wire Slave Serial Bus (I2C)** | | | |
| 47 | XSSDA | DIO | 2-wire slave serial data<br>Programmable 3.3V/5V tolerant bidirectional buffer, pull-down |
| 48 | XSSCL | DIO | 2-wire slave serial clock<br>Programmable 3.3V/5V tolerant bidirectional buffer, pull-down |
| **Miscellaneous** | | | |
| 8 | RREF | AI | Connect external reference resistor (12KΩ±1%) |
| 16 | XPWDN | DO | External device power down control signal (default tri-state)<br>Programmable 3.3V/5V tolerance output buffer |
| 46 | XRSTO | DO | External codec reset (default tri-state)<br>Programmable 3.3V/5V tolerance output buffer |
| 80 | XSELF_PWR | DI | Self Power used, 1:self power, 0:bus power<br>Programmable 3.3V input buffer, Schmitt trigger, Pull-down |
| 2 | XRST | DI | CM6210 chip reset |
| 3 | XTEST | DI | Test mode select pin:<br>H: Test Mode<br>L: Normal Operation |

# 6 Electrical Characteristics

## 6.1 Maximum Ratings

**Test conditions; $V_{DD}$ = 3.3V, DGND =0V, TA=+25°C**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Storage temperature | - | -55 | - | 150 | oC |
| Operating ambient temperature | - | 0 | 25 | 75 | oC |
| DC supply voltage | - | 3.0 | 3.3 | 3.6 | V |
| I/O pin voltage | - | GND | - | VDD | V |
| Power dissipation | - | - | 0.15 | - | W |

## 6.2 Recommended Operation Conditions

**Test conditions: VDD = 3.3V, DGND =0V, TA=+25°C**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Input voltage range | - | $V_{DD}$-0.3 | $V_{DD}$ | $V_{DD}$+0.3 | V |
| Output voltage range | - | 0 | - | $V_{DD}$ | V |

## 6.3 Power Consumption

**Test conditions: DVDD = 3.3V, DGND =0V, TA=+25°C**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Supply current : power up | - | - | 79.42 | - | mA |
| Supply current : power down | - | - | 0.163 | - | uA |

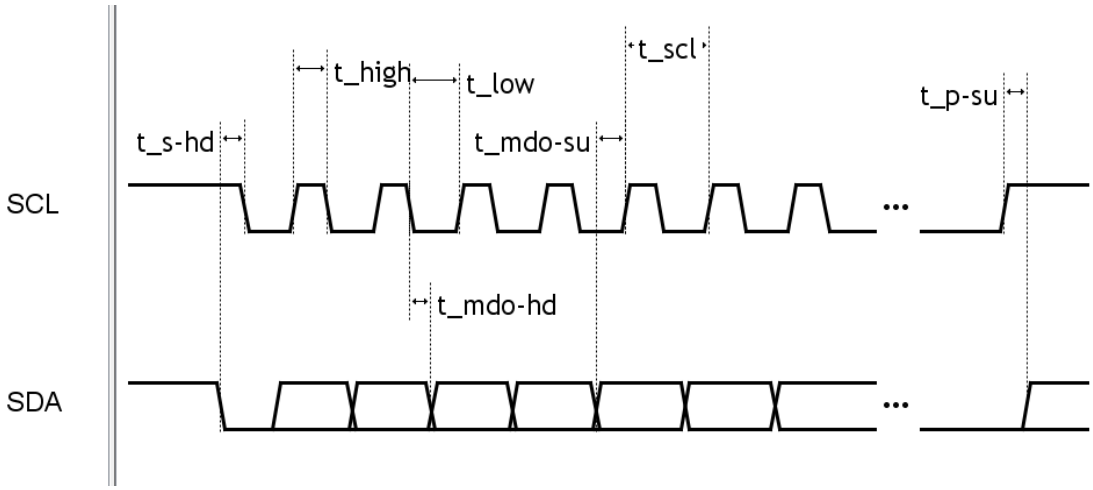
## 6.4 DC Characteristics

**Test Conditions: DVDD = 3.3V, DGND =0V, TA=+25°C**

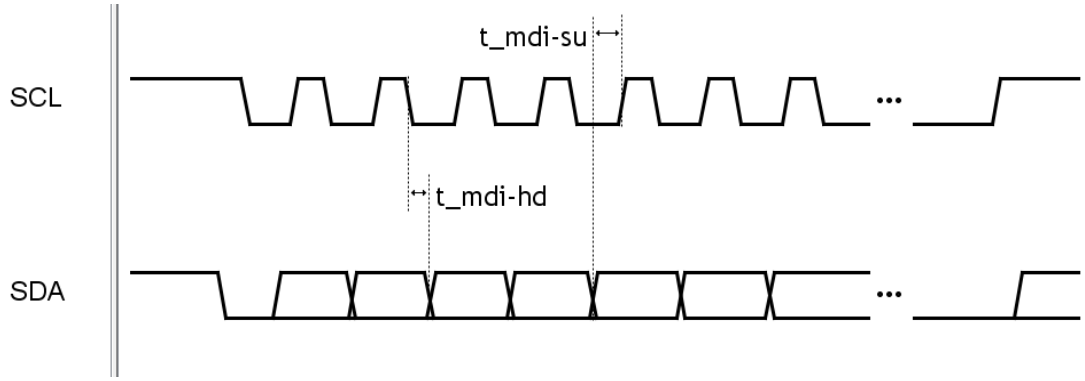
| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Input voltage range | Vin | $V_{DD}$-0.3 | $V_{DD}$ | $V_{DD}$+0.3 | V |
| Output voltage range | Vout | 0 | - | $V_{DD}$ | V |
| High level input voltage | Vih | 0.7$V_{DD}$ | - | - | V |
| Low level input voltage | Vil | - | - | 0.3$V_{DD}$ | V |
| High level output voitage | Voh | 2.4 | - | - | V |
| Low level output voltage | Vol | | - | 0.4 | V |
| Input leakage current | Iil | -10 | - | 10 | uA |
| Output leakage current | Iol | -10 | - | 10 | uA |
| Output buffer driver current | - | - | 8 | - | mA |
| SPDIF transmit output driver current | - | - | 8 | - | mA |

## 6.5 I/O Timing

### 6.5.1 I2C Master Interface




(a) I2C master data out




(b) I2C master data in

**Fig. 6.1 I2C standard mode and fast mode timing (a) master data out (b) master data in.**

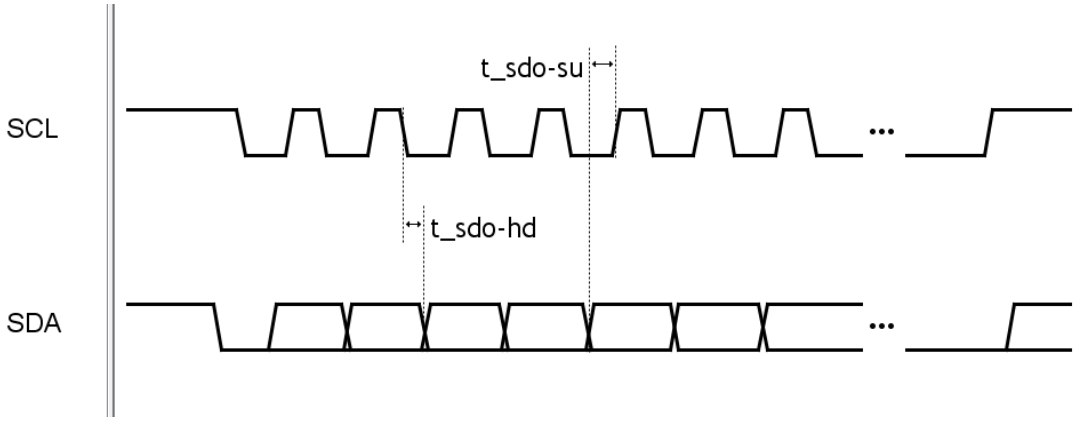
**Standard mode**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| SCL clock frequency | f_scl | - | 95.238 | - | KHz |
| SCL clock period | t_scl | - | 10.5 | - | us |
| Low period of SCL clock | t_low | 5.67 | - | - | us |
| High period of SCL clock | t_high | 3.78 | - | - | us |
| Hold time for START condition | t_s-hd | 3.78 | - | - | us |
| Setup time for STOP condition | t_p-su | 3.78 | - | - | us |
| Master DataOut setup time | t_mdo-su | | - | 3.78 | us |
| Master DataOut hold time | t_mdo-hd | | - | 1.89 | us |
| Master DataIn setup time | t_mdi-su | 1 | - | - | ns |
| Master DataIn hold time | t_mdi-hd | 1 | - | - | ns |

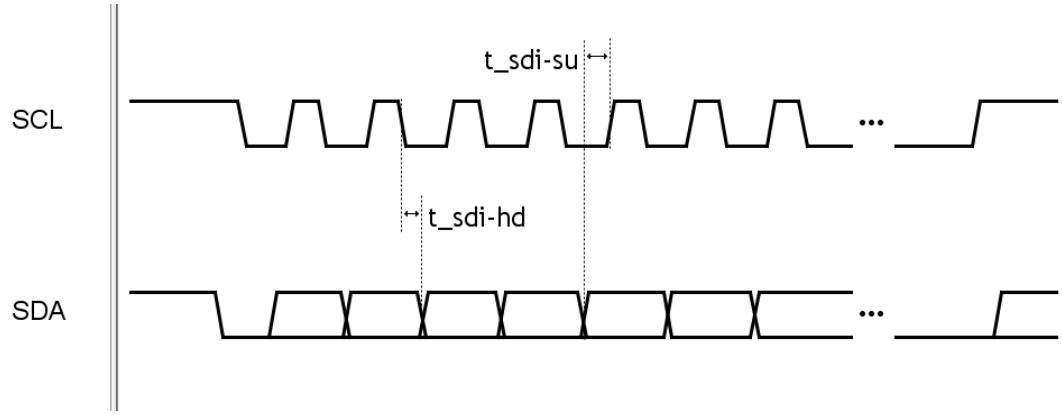
**Fast mode**

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| SCL clock frequency | f_scl | - | 375 | - | KHz |
| SCL clock period | t_scl | - | 2.6667 | - | us |
| Low period of SCL clock | t_low | 1.44 | - | - | us |
| High period of SCL clock | t_high | 0.96 | - | - | us |
| Hold time for START condition | t_s-hd | 0.96 | - | - | us |
| Setup time for STOP condition | t_p-su | 0.96 | - | - | us |
| Master DataOut setup time | t_mdo-su | - | - | 0.96 | us |
| Master DataOut hold time | t_mdo-hd | - | - | 0.48 | us |
| Master DataIn setup time | t_mdi-su | 1 | - | - | ns |
| Master DataIn hold time | t_mdi-hd | 1 | - | - | ns |

### 6.5.2 I2C Slave Interface




(a) I2C slave data out




(b) I2C slave data in

**Fig. 6.2 I2C slave standard mode and fast mode timing (a) slave data out (b) slave data in.**

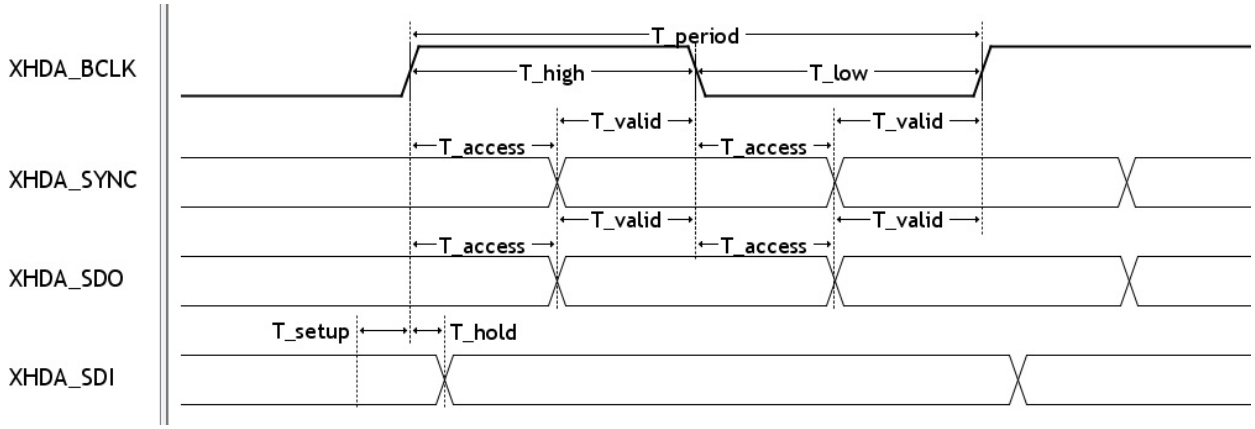
**Standard mode**

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Slave DataOut setup time | t_sdo-su | - | 5.19 | us |
| Slave DataOut hold time | t_sdo-hd | - | 0.48 | us |
| Slave DataIn setup time | t_sdi-su | 37 | - | ns |
| Slave DataIn hold time | t_sdi-hd | 1 | - | ns |

**Fast mode**

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Slave DataOut setup time | t_sdo-su | - | 0.9617 | us |
| Slave DataOut hold time | t_sdo-hd | - | 0.4781 | us |
| Slave DataIn setup time | t_sdi-su | 37 | - | ns |
| Slave DataIn hold time | t_sdi-hd | 1 | - | ns |

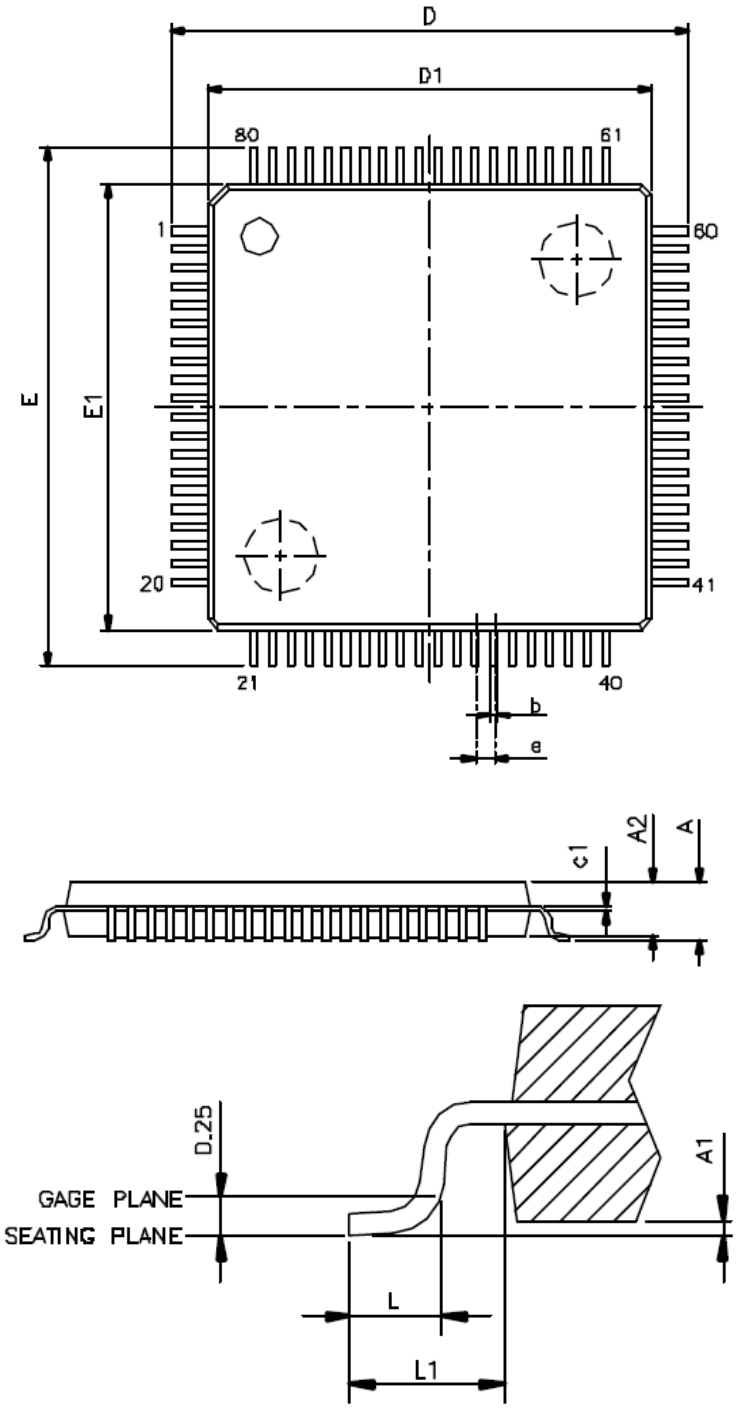
### 6.5.3 HDA Interface




| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| XHDA_BCLK frequency | | 23.99 | 24 | 24.0024 | ns |
| Total period of XHDA_BCLK | T_period | 41.363 | 41.67 | 41.971 | ns |
| High phase of XHDA_BCLK | T_high | 18.75 | | 22.91 | ns |
| Low phase of XHDA_BCLK | T_low | 18.75 | | 22.91 | ns |
| XHDA_BCLK jitter | | | 150 | 300 | ns |
| Time duration for which XHDA_SDO is valid after the XHDA_BCLK edge | T_access | 11 | | 11 | ns |
| Data Valid Time | T_valid | 7.75 | | 11.91 | ns |
| Setup for XHDA_SDI at rising edge of the XHDA_BCLK | T_setup | 7 | | | ns |
| Hold for XHDA_SDI at rising edge of the XHDA_BCLK | T_hold | 2 | | | ns |

# 7 Package Dimensions

**LQFP-80 (10 x 10 mm)**



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | MAX. |
|---|---|---|
| A | -- | 1.6 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| c1 | 0.09 | 0.16 |
| D | 12 BSC | |
| D1 | 10 BSC | |
| E | 12 BSC | |
| E1 | 10 BSC | |
| e | 0.4 BSC | |
| b | 0.17 | 0.27 |
| L | 0.45 | 0.75 |
| L1 | 1 REF | |

NOTES:
1. JEDEC OUTLINE:MS-026 BCE
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

## —End of Datasheet—

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