



GSV1011

HDMI1.4 HDCP1.4 Repeater with TTL/LVDS
Input/Output and Audio Extraction/Insertion

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PRODUCT SPECIFICATION

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1 General Information

1.1 General Information

The GSV1011 is a HDMI1.4 compatible TRX transceiver with LVDS/TTL data bus, and supports HDCP 1.4. For audio extraction and insertion, GSV1011 can support up to 8-channel I2S/2-channel S/PDIF/TDM.

The HDMI input maximum processing pixel clock frequency is 300MHz which means the video resolution can support up to 4kx2k@30Hz 4:4:4 8-bit. The maximum processing audio sample frequency is 8-channel 192K Hz for non-compression timing.

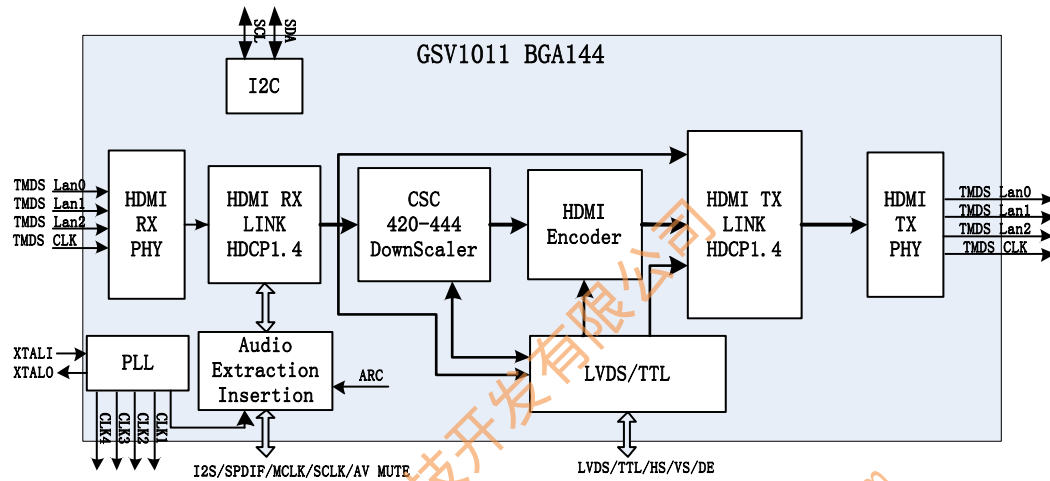


Figure 1 top diagram

Internal video processing supports CSC/ Dither/ 420<->444 conversion/ Downscaler/ Deinterlacer/ LVDS and TTL Pin Mapping. Figure 2 is its diagram.

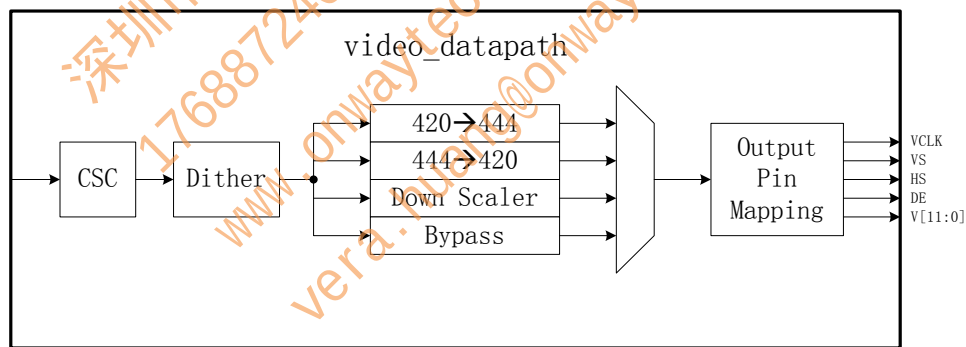


Figure 2 video datapath diagram

Audio TTL output pins support audio format listed in Table 1.

Table 1 supported audio format

Packet ID	Packet Type	Sample Frequency or Frame Rate		
		32.0, 44.1, 48.0, 88.2, 96.0, 176.4, and 192.0 kHz	256.0, 352.8, 384.0, 512.0, 705.6, 768.0 kHz	64.0 and 128.0 kHz
0x02	Audio Sample (L-PCM and IEC 61937 compressed formats)	Y	N	Y
0x07	One Bit Audio Sample Packet	Y	N	N
0x08	DST Audio Packet	Y	N	N
0x09	High Bitrate Audio Stream Packet (IEC 61937)	N	Y	N

An internal Clock Generator can be used to generate 4 independent output clocks, which will greatly remove complexity of using dedicated clock device.

1.2 Features

1.2.1 HDMI TRX transceiver

- Compliant with HDMI1.4b
- Compliant with HDCP1.4
- Data rate up to 18Gbps
- Programmable HDMI Tx output swing, slew-rate, pre-emphasis
- Adaptive receiver equalization
- AC-coupling capable
- UDP bus to support the combination of video/audio/info-frames
- Color Space Converter supports any conversion between different color spaces
- HDR supported (HDR10/HDR12/Dolby Vision/HLG)
- 5V tolerance on DDC/HPD/CEC
- Up to 4 channel clock generators, ranging 25MHz~600MHz

1.2.2 Multi-Port LVDS Transmitter/Receiver

- Bi-directional LVDS, supports video format up to 4K 30 444
- Compatible with series FPGAs' LVDS standard (15 pairs in maximum)
 - ◆ Programmable output swing, slew-rate, common voltage and pre-emphasis
 - ◆ SDR/DDR/xN (N = 1~7) LVDS Clock transmitter with configurable output phase
 - ◆ Data rate up to 1.5Gbps per lane
 - ◆ Differential HS/VS/DE available
 - ◆ Embedded SAV/EAV mode supported
- Compatible with VESA and JEIDA standards
 - ◆ Single/Dual-Port LVDS Transmitter
 - ◆ Programmable output swing, slew-rate, common voltage and pre-emphasis
 - ◆ Data rate up to 1.5Gbps per lane

1.2.3 Compatible TTL Transmitter/Receiver

- 48bit TTL Video Output
 - ◆ Programmable drive strength, slew-rate, driver disabled state control
 - ◆ SDR/DDR Clock Output with configurable output phase
 - ◆ Data rate up to 300Mbps per lane
 - ◆ HS/VS/DE available
 - ◆ Embedded SAV/EAV mode supported
 - ◆ 1.8/2.5/3.3V VCCO compatible.
- 48bit TTL Video Receiver
 - ◆ TTL Schmitt trigger receiver and CMOS receiver selectable
 - ◆ SDR/DDR Clock Input available with 0 degree or 90 degree

5 Package Information

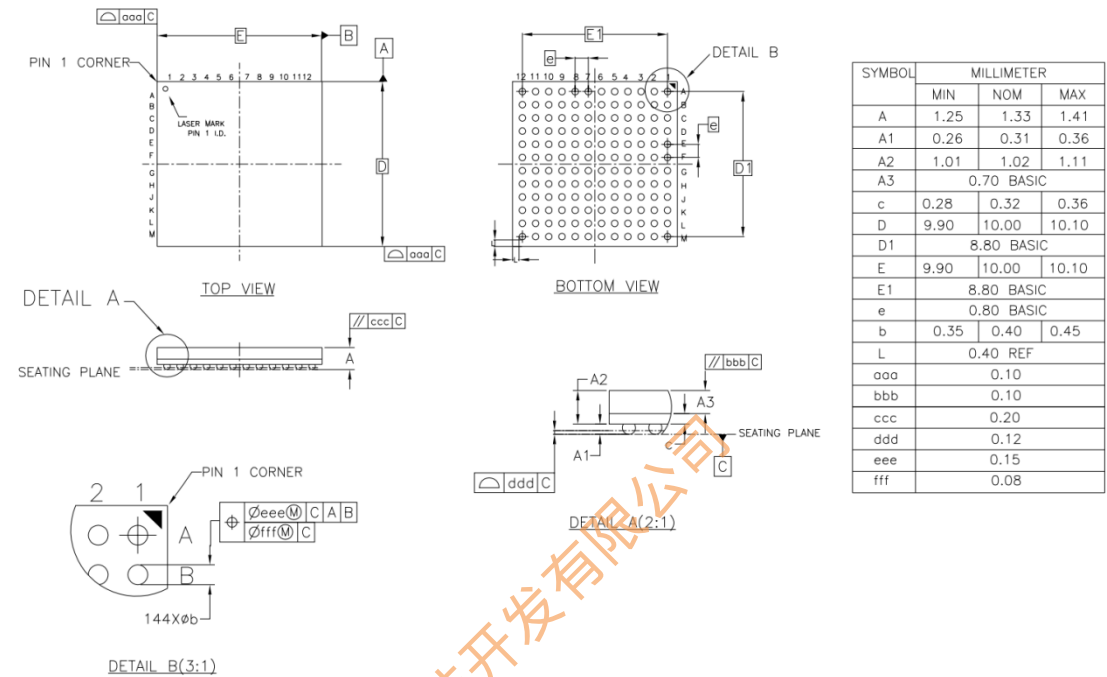


Figure 28. Package Dimensions (BGA144)

6 Ordering Guide

Table 42. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV1011	−20 °C to +85 °C	BGA144, 0.8 mm ball pitch, 10 mm x 10 mm outline	Tray

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