GSV2015

HDMI2.0 Receiver with TTL/LVDS Output and Audio Extraction

September, 2019

PRODUCT SPECIFICATION

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1 General Information

1.1 General Information

The GSV2015 is a HDMI1.4/2.0 compatible RX receiver with LVDS/TTL data bus, and supports HDCP 1.4/2.2. For audio extraction and insertion, GSV2015 can support up to 8-channel I2S/2-channel S/PDIF/TDM.
The HDMI input maximum processing pixel clock frequency is 600MHz which means the video resolution can support up to 4kx2k@60Hz 4:4:4 8-bit. The maximum processing audio sample frequency is 8-channel 192K Hz for non-compression timing.

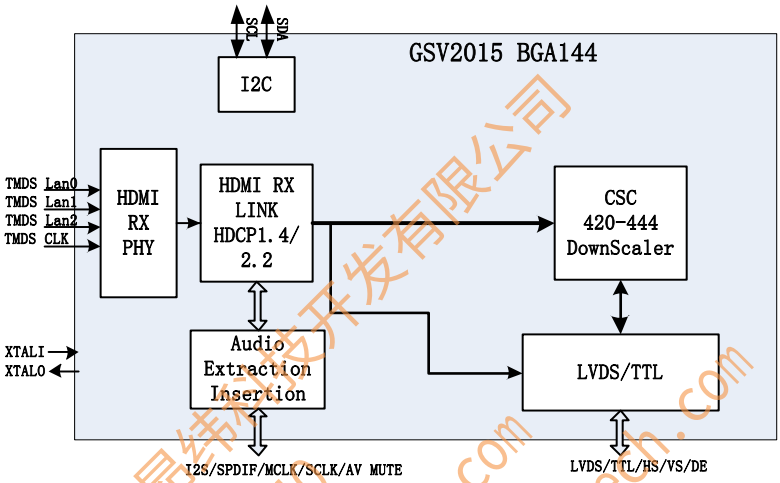

Figure 1. Top Diagram

Internal video processing supports CSC/ Dither/ 420<->444 conversion/ Downscaler/ Deinterlacer/ LVDS and TTL Pin Mapping. Figure 2 is its diagram.

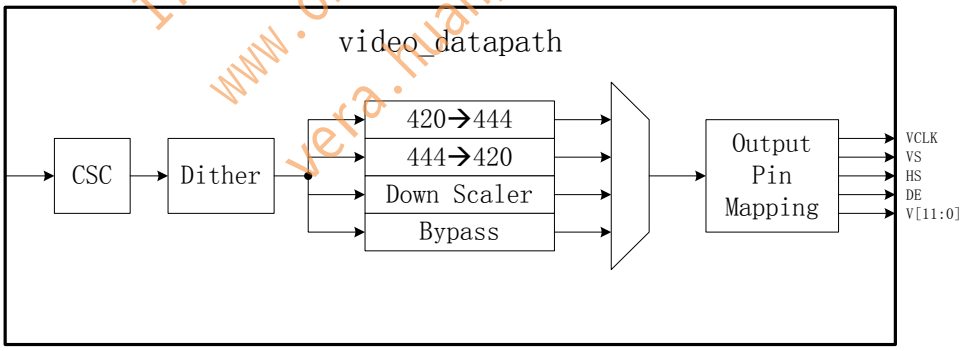

Figure 2. Video Datapath

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Audio TTL output pins support audio format listed in Table 1.

Table 1. Supported Audio Format

Packet ID	Packet Type	Sample Frequency or Frame Rate		
		32.0, 44.1, 48.0, 88.2, 96.0, 176.4, and 192.0 kHz	256.0, 352.8, 384.0, 512.0, 705.6, 768.0 kHz	64.0 and 128.0 kHz
0x02	Audio Sample (L-PCM and IEC 61937 compressed formats)	Y	N	Y
0x07	One Bit Audio Sample Packet	Y	N	N
0x08	DST Audio Packet	Y	N	N
0x09	High Bitrate Audio Stream Packet (IEC 61937)	N	Y	N

An internal Clock Generator can be used to generate 4 independent output clocks, which will greatly remove complexity of using dedicated clock device.

1.2 Features

1.2.1 HDMI RX Receiver

- Compliant with HDMI2.0b, HDMI1.4b
- Compliant with HDCP2.2/2.3 and HDCP1.4
- Data rate up to 18Gbps
- Adaptive receiver equalization
- AC-coupling capable
- UDP bus to support the combination of video/audio/info-frames
- Color Space Converter supports any conversion between different color spaces
- HDR supported (HDR10/HDR12/Dolby Vision/HLG)
- 5V tolerance on DDC/HPD/CEC

1.2.2 Multi-Port LVDS Transmitter

- Bi-directional LVDS, supports video format up to 4K 60 444
- Compatible with series FPGAs' LVDS standard (15 pairs in maximum)
  - Programmable output swing, slew-rate, common voltage and pre-emphasis
  - SDR/DDR/xN (N = 1~7) LVDS Clock transmitter with configurable output phase
  - Data rate up to 1.5Gbps per lane
  - Differential HS/VS/DE available
  - Embedded SAV/EAV mode supported
- Compatible with VESA and JEIDA standards
  - Single/Dual-Port LVDS Transmitter
  - Programmable output swing , slew-rate , common voltage and pre-emphasis
  - Data rate up to 1.5Gbps per lane

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1.2.3 Compatible TTL Transmitter

- 48-bit TTL Video Output
  - Programmable drive strength, slew-rate, driver disabled state control
  - SDR/DDR Clock Output with configurable output phase
  - Data rate up to 300Mbps per lane
  - HS/VS/DE available
  - Embedded SAV/EAV mode supported
  - 1.8/2.5/3.3V VCCO compatible.

1.2.4 Audio Input/Output

- SPDIF/I2S/HBR/DSD/TDM Audio Extraction

1.3 Chip Application Modes

1.3.1 HDMI 2.0 RX with LVDS/TTL output mirroring input

The LVDS/TTL Output are mirrored from input with no internal processing. Downscaler/444-420 converter can be used to guarantee the HDMI Tx has the best 4K/2K compatibility with fixed HDMI Rx input timing.

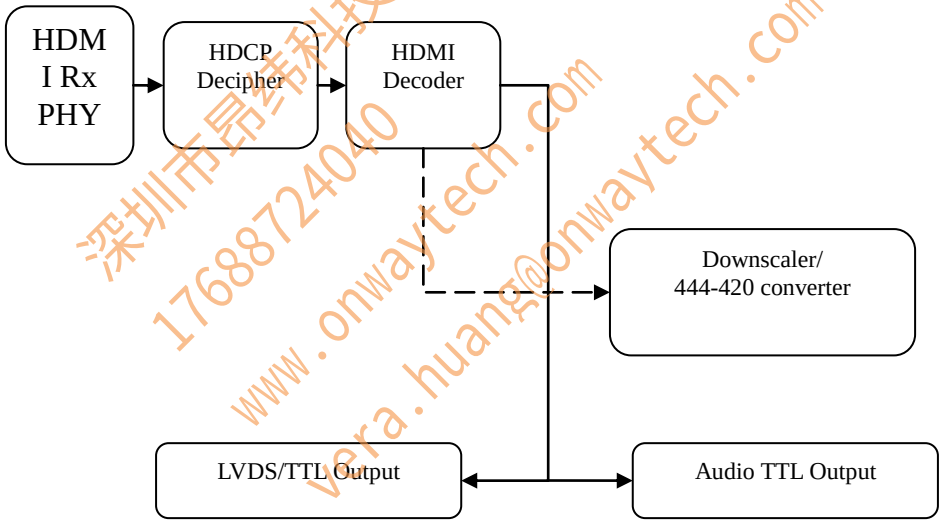

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Figure 3. HDMI 2.0 RX with LVDS/TTL output mirroring input

1.3.2 HDMI 2.0 RX with LVDS/TTL output using UDP mode

Patented UDP mode is used to combine input video/audio together onto a single universal bus to minimize the pin number.

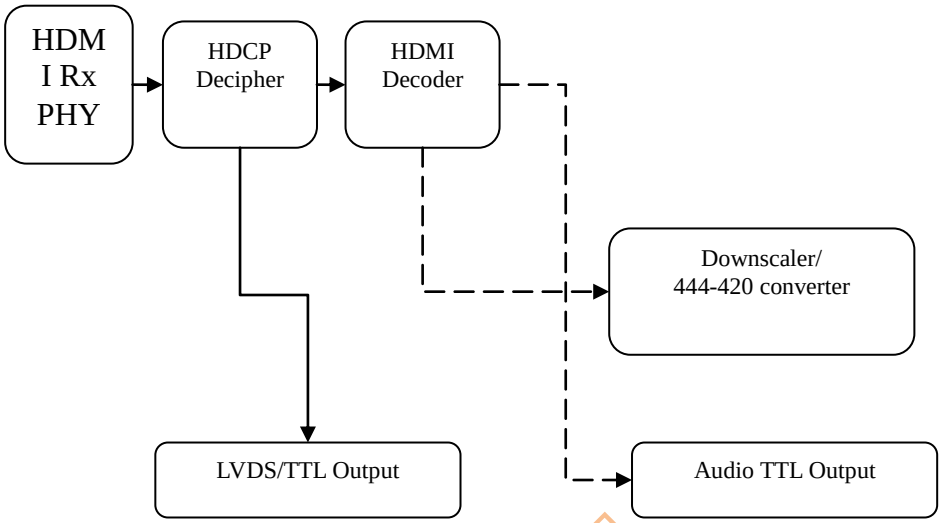


Figure 4. HDMI 2.0 RX with LVDS/TTL output using UDP mode

1.3.3 HDMI 2.0 RX with LVDS/TTL output in single color space

Internal IPs could be used to do color space conversion to guarantee the LVDS/TTL output is always in the same color space (either RGB/YCbCr 444/YCbCr422/YCbCr420). If needed, this mode can also downscale all the 4K to 2K for LVDS/TTL Output. This application mode is often used in embedded sync transmission.

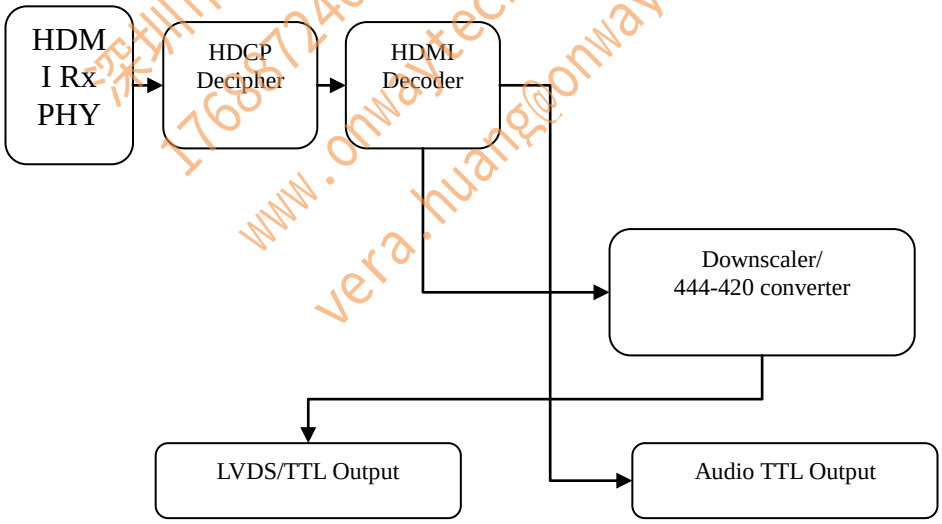
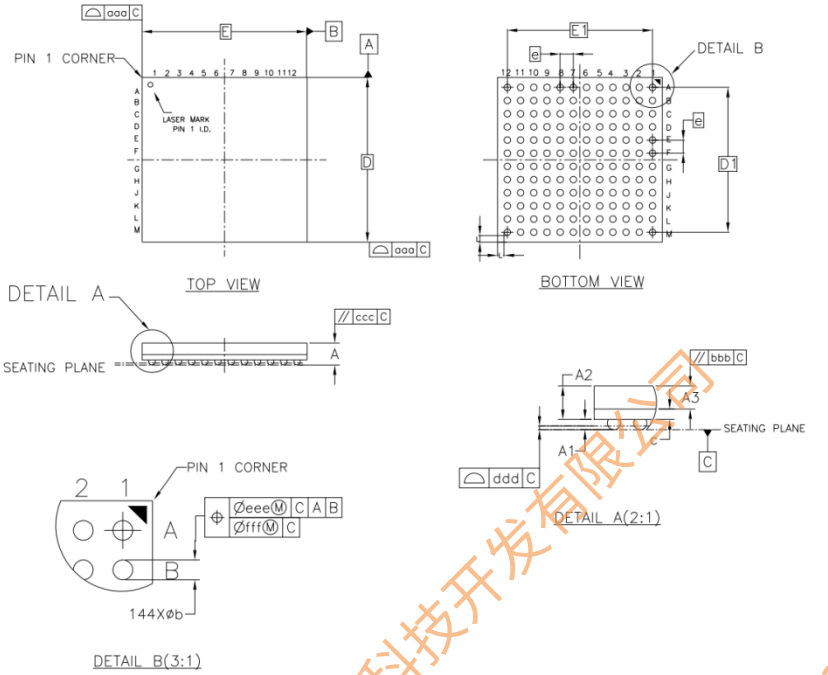


Figure 5. HDMI 2.0 RX with LVDS/TTL output in single color space

1.4 Audio Bus Output Capability

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. Normal Pin Setting is as below.

5 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.25	1.33	1.41
A1	0.26	0.31	0.36
A2	1.01	1.02	1.11
A3		0.70 BASIC	
c	0.28	0.32	0.36
D	9.90	10.00	10.10
D1		8.80 BASIC	
E	9.90	10.00	10.10
E1		8.80 BASIC	
e		0.80 BASIC	
b	0.35	0.40	0.45
L		0.40 REF	
aaa		0.10	
bbb		0.10	
ccc		0.20	
ddd		0.12	
eee		0.15	
fff		0.08	

Figure 24. Package Dimensions (BGA144)

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6 Ordering Guide

Table 38. Ordering Infomation

Part Number.	Temperature Range	Package Description	Packing Type
GSV2015	−20 ℃ to +85 ℃	BGA144, 0.8 mm ball pitch, 10 mm x 10 mm outline	Tray

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