GSV6127C

Type-C/DisplayPort 1.4/HDMI 2.0 to MIPI CSI-2 Mixed Converter with Embedded MCU

Oct, 2022

Preliminary Product Specification

1. General Description

1.1 General Information

Gscoolink GSV6127C is a high-performance, low-power DisplayPort 1.4/ HDMI 2.0 to MIPI CSI-2 mixed converter. By integrating enhanced microcontroller, GSV6127C has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver supports up to 32.4Gbps (HBR3, 4-lane), HDMI Receiver supports up to 18Gbps (TMDS, 6G/3Lane). With embedded Channel Configuration (CC), Power Delivery (PD) controller and Billboard USB 2.0 controller, GSV6127C can support Type-C Alternate DisplayPort for Type-C to MIPI bridge application. The superior architecture of GSV6127C provides economical smaller footprint solutions using QFN76, targeting for low power embedded applications.

HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV6127C for its DisplayPort and HDMI port. Color Space Conversion, 420-444/422 Conversion, De-Interlacer and Downscaler are supported for flexible video processing. Audio Extraction of HDMI Rx and DisplayPort Rx is supported in GSV6127C for audio processing. With audio sample raw data detection feature, LPCM channel filled with consistent zero raw sample data will be automatically detected and muted.

Within 4kV HBM tolerance, GSV6127C's operation temperature range is -40 ºC to 85 ºC using automotive qualified process. An internal Video Generator can be used to generate any uncompressed video timing defined in DisplayPort HBR3 bandwidth, such as 4K@60Hz, 4K@30Hz, 480i@60Hz.

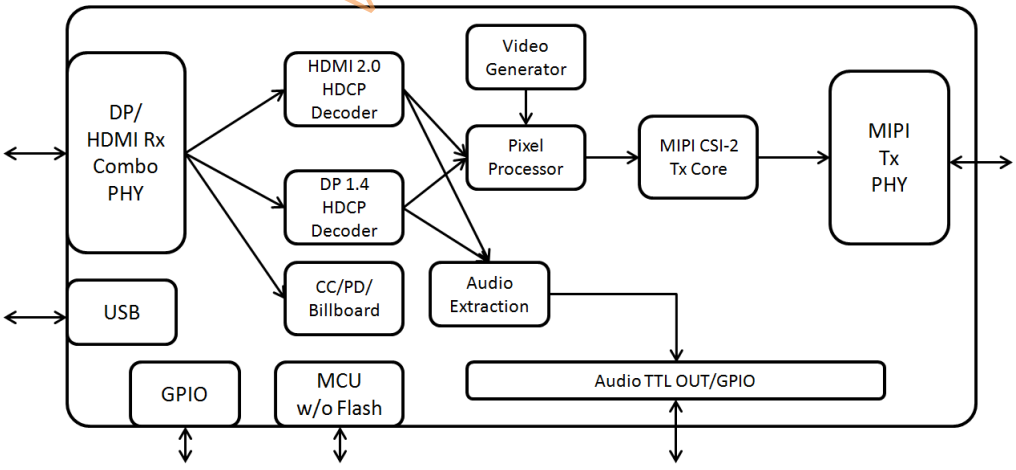


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Extraction
- Support Horizontal Blanking Expansion up to 4K@60Hz format
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)
- 3D format support of frame sequential, stacked frame, side-by-side, top-to-bottom

1.2.2 HDMI Receiver

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Embedded arbitrary EDID (up to 512 bytes)

- 5V tolerance on DDC/HPD pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.3 MIPI CSI-2 Transmitter

- Support MIPI CSI-2 v3.0 version transmission using D-PHY or C-PHY interface
- Support 2.5G bps 1/2/4/8-lane MIPI D-PHY Out
- Support 5.7G bps 1/2/3-lane MIPI C-PHY Out
- Programmable output swing , slew-rate and pre-emphasis
- CSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

1.2.4 USB Type-C DisplayPort Alternative Mode Receiver

- Compliant with USB Type-C 1.1/1.0 Specification
- Compliant with USB Power Delivery 3.0 Specification
- Programmable USB Type-C Channel Configuration function
- Support Billboard in USB 2.0

1.2.5 Pixel Processor

- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with fixed horizontal and vertical 2 ratio for 4K to 2K conversion
- Deinterlacer for interlaced timing

1.2.6 Audio Output

- I2S and SPDIF Audio Extraction from HDMI Rx/ DisplayPort Rx /Type-C Rx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction

1.2.7 System Features

- Optional External MCU (via I2C)/ Internal MCU mode

- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 Type-C Alt-Mode to MIPI CSI-2 Conversion

RxPort is configured as Type-C Alt-Mode (DisplayPort) Rx Input. Together with on-chip CC, USB 2.0 IP support, Type-C USB input can be configured to DisplayPort 1.4a input stream for processing. This mode is designed for Type-C to SoC MIPI panel front-end interconnection. D-PHY or C-PHY interface interconnection are both applicable based on application designs.

With internal Color Space Converter, De-Interlacer, DisplayPort input timing can be converted to MIPI compatible output timing. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

Meanwhile, Audio extraction can be applicable if required.

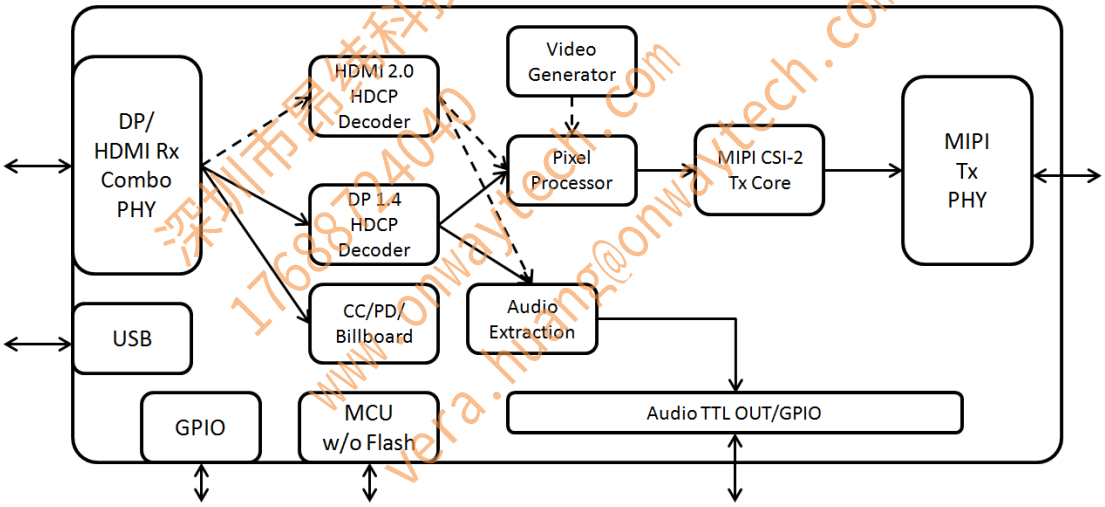


Figure 2. Type-C Alt-Mode to MIPI CSI-2 Application

1.3.2 HDMI 2.0 to MIPI CSI-2 Conversion

RxPort is configured as HDMI 2.0 Input. This mode is designed for HDMI 2.0 to SoC MIPI panel front-end interconnection.

With internal Color Space Converter, De-Interlacer, HDMI 2.0 input timing can be converted to MIPI compatible output timing. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream

capability.

Meanwhile, Audio extraction can be applicable if required.

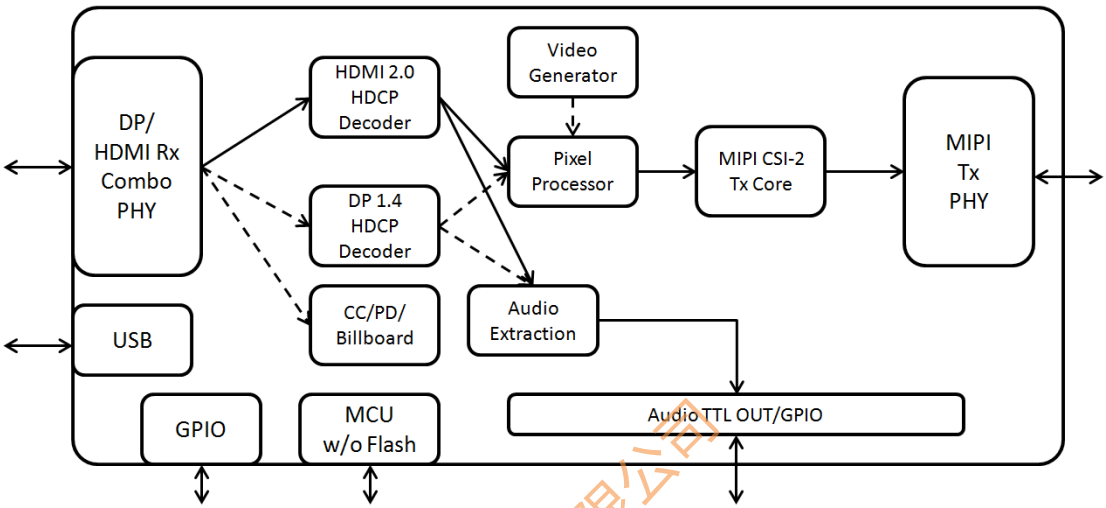


Figure 3. HDMI 2.0 to MIPI CSI-2 Application

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. General configuration of pin settings is shown below:

Table 2. I2S Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Output	Fixed to 64Fs
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs

SPDIF is also capable of sending out with by configuring to AUD_D0 pins. So in GSV6127C application, AUD1 group bus can be used to extract I2S while AUD2_D0 can be used to extract SPIDF.

Table 3. SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF[0]	Output	SPDIF Data[0], 1/2 channels

2. Pin Description

2.1 Pin Diagram

QFN76 Pin definition is defined as below.

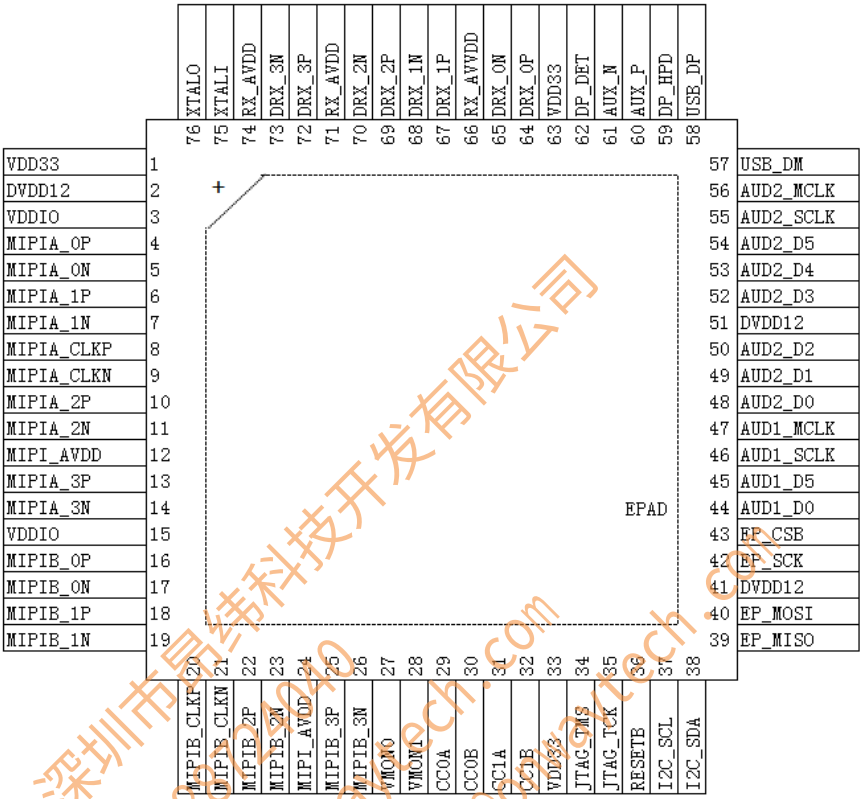


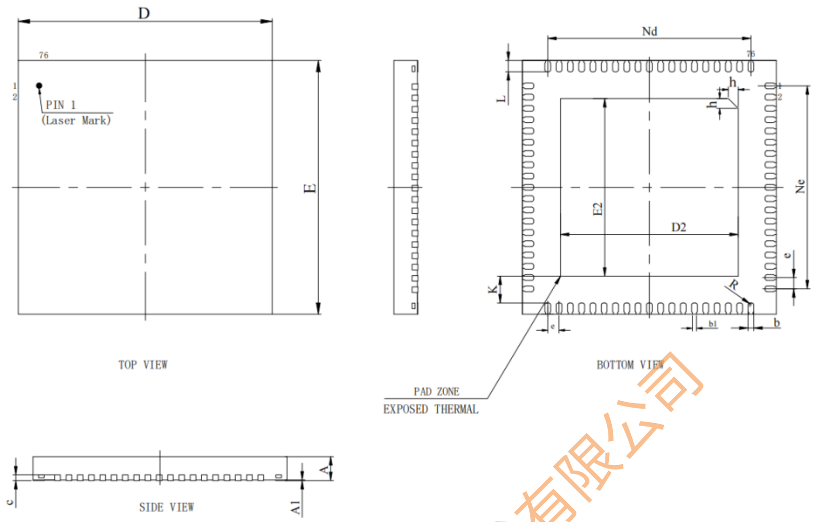
Figure 4. GSV6127C QFN76 Pin Diagram

2.2 QFN76 Pin Description

Table 4. QFN76 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI RX Pins/Type-C UFP/DisplayPort RX Pins			
DP_DET	I	62	HDMI: RX 5V Detection PAD DP: RX DP Detection PAD
DP_HPD	O	59	HDMI: RX HPD PAD DP: RX HPD PAD
AUX_P	I/O	60	HDMI: RX DDC SDA PAD DP: RX AUX_P PAD
AUX_N	I/O	61	HDMI: RX DDC SCL PAD DP: RX AUX_N PAD

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
• A	0.80	0.85	0.90
• A1	0.00	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.203REF		
• D	8.90	9.00	9.10
D2	6.20	6.30	6.40
e	0.40BSC		
Nd	7.20BSC		
• E	8.90	9.00	9.10
E2	6.20	6.30	6.40
Ne	7.20BSC		
L	0.35	0.40	0.45
K	0.95REF		
R	0.075REF		
h	0.30	0.35	0.40

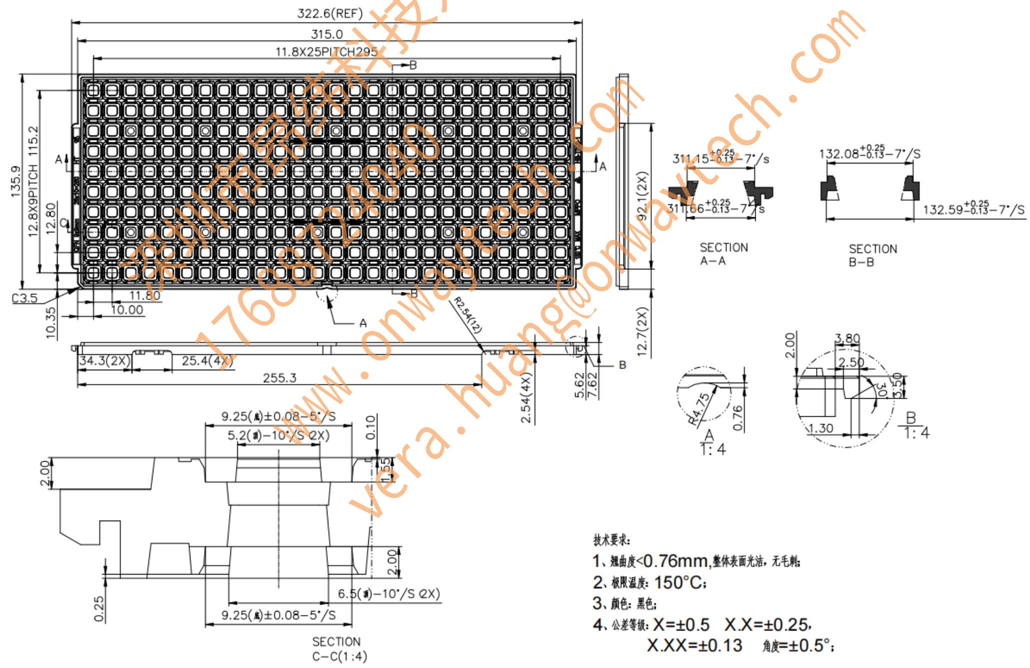


Figure 8. Package Dimensions (QFN76)

5. Ordering Guide

Table 14. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV6127C	−40°C to +85°C	QFN76	Tray