GSV6127X

Type-C/DisplayPort 1.4/HDMI 2.0 and Bi-Directional MIPI/LVDS/TTL Mixed Converter with Embedded MCU

Oct, 2022

Product Specification

1. General Description

1.1 General Information

Gscoolink GSV6127X is a high-performance, low-power DisplayPort 1.4/ HDMI 2.0 to MIPI CSI-2/LVDS/TTL mixed converter. With Dual Port MIPI interface, genuine 4K60 444 can be transmitted using MIPI interface. By integrating enhanced microcontroller, GSV6127X has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver supports up to 32.4Gbps (HBR3, 4-lane), HDMI Receiver supports up to 18Gbps (TMDS, 6G/3Lane). With embedded Channel Configuration (CC), Power Delivery (PD) controller and Billboard USB 2.0 controller, GSV6127X can support Type-C Alternate DisplayPort to MIPI bridge or MIPI to Type-C Alternate DisplayPort application. The superior architecture of GSV6127X provides economical smaller footprint solutions using QFN96, targeting for low power embedded applications.

HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV6127X for its DisplayPort and HDMI port. Color Space Conversion, 420-444/422 Conversion, De-Interlacer and Downscaler are supported for flexible video processing. Audio Extraction of HDMI Rx and DisplayPort Rx is supported in GSV6127X for audio processing. With audio sample raw data detection feature, LPCM channel filled with consistent zero raw sample data will be automatically detected and muted.

Within 4kV HBM tolerance, GSV6127X's operation temperature range is -40 ºC to 85 ºC using automotive qualified process.

An internal Video Generator can be used to generate any uncompressed video timing defined in DisplayPort HBR3 bandwidth, such as 4K@60Hz, 4K@30Hz, 480i@60Hz.

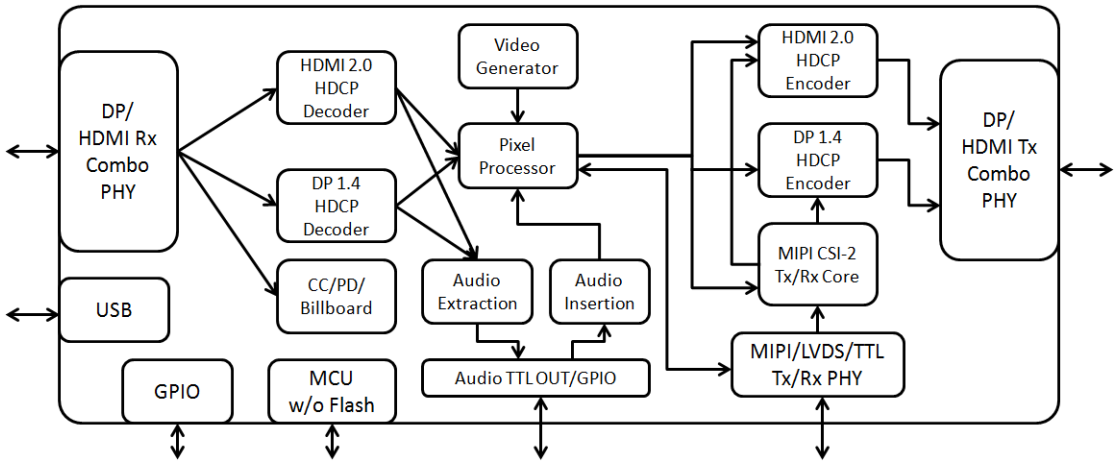


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Extraction
- Support Horizontal Blanking Expansion up to 4K@60Hz format
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)

- 3D format support of frame sequential, stacked frame, side-by-side, top-to-bottom

1.2.2 HDMI Receiver

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.3 DisplayPort Transmitter

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Insertion
- Support Horizontal Blanking Reduction up to 4K@60Hz format
- Support Spread Spectrum Clock (SSC)
- 3D format support of stacked frame, side-by-side, top-to-bottom

1.2.4 HDMI Transmitter Features

- Compliant with HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 18Gbps (TMDS 6Gbps/3 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS input/output
- Support Color Space Converter in TMDS mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync

- Support ALLM
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

1.2.5 MIPI CSI-2/DSI-2 Transmitter/Receiver

- Support MIPI CSI-2 v3.0 version transmission using D-PHY or C-PHY interface
- Support MIPI CSI-2 v3.0 version receiving using D-PHY interface
- Support MIPI DSI-2 v2.0 version receiving using D-PHY interface
- Support 2.5G bps 1/2/3/4-lane MIPI D-PHY In/Out
- Support 5.7G bps 1/2/3-lane MIPI C-PHY Out
- Programmable output swing , slew-rate and pre-emphasis
- CSI-2/DSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

1.2.6 Multi-Port LVDS Transmitter/Receiver

- Bi-directional LVDS, supports video format up to 4K60 420 12-bit
  - 4K60 RGB/YCbCr444/YCbCr422 will be converted to YCbCr420
- Compatible with series FPGAs' LVDS standard (12 pairs in maximum)
  - Programmable output swing, slew-rate, common voltage and pre-emphasis
  - SDR/DDR/xN (N = 1~7) LVDS Clock transmitter with configurable output phase
  - Data rate up to 1.5Gbps per lane
  - Differential HS/VS/DE available
  - Embedded SAV/EAV mode supported
- Compatible with VESA and JEIDA standards
  - Single/Dual-Port LVDS Transmitter
  - Programmable output swing , slew-rate , common voltage and pre-emphasis
  - Data rate up to 1.5Gbps per lane

1.2.7 Compatible TTL Transmitter/Receiver

- 24-bit TTL Video Receiver up to 1080p60 24-bit
  - TTL Schmitt trigger receiver and CMOS receiver selectable

- SDR/DDR Clock Input available with 0 degree or 90 degree
- Data rate up to 150Mbps per lane
- HS/VS/DE available
- Embedded SAV/EAV mode supported

1.2.8 USB Type-C DisplayPort Alternative Mode Transceiver

- Compliant with USB Type-C 1.1/1.0 Specification
- Compliant with USB Power Delivery 3.0 Specification
- Programmable USB Type-C Channel Configuration function
- Support Billboard in USB 2.0

1.2.9 Pixel Processor

- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with fixed horizontal and vertical 2 ratio for 4K to 2K conversion
- Deinterlacer for interlaced timing

1.2.10 Audio Output and Input

- I2S and SPDIF Audio Extraction from HDMI Rx/ DisplayPort Rx /Type-C Rx
- I2S and SPDIF Audio Insertion to HDMI Tx/ DisplayPort Tx /Type-C Tx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction

1.2.11 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 Type-C Alt-Mode In to HDMI Out with MIPI Out Application

RxPort is configured as Type-C Alt-Mode (DisplayPort) Rx Input. Together with on-chip CC, USB 2.0 IP support, Type-C USB input can be configured to DisplayPort 1.4a input stream for processing. This mode is designed for Type-C to SoC MIPI panel front-end interconnection. If required, the MIPI interface can also be set to LVDS/TTL for output (up to 4K60 420 timing). D-PHY or C-PHY interface interconnection are both applicable based on application designs. TxPort can be configured as DisplayPort or HDMI Output. When HDMI output is used for loop back, the application can also be considered as DisplayPort to HDMI converter.

With internal Color Space Converter, De-Interlacer, DisplayPort input timing can be converted to MIPI compatible output timing. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

Meanwhile, Audio extraction can be applicable if required.

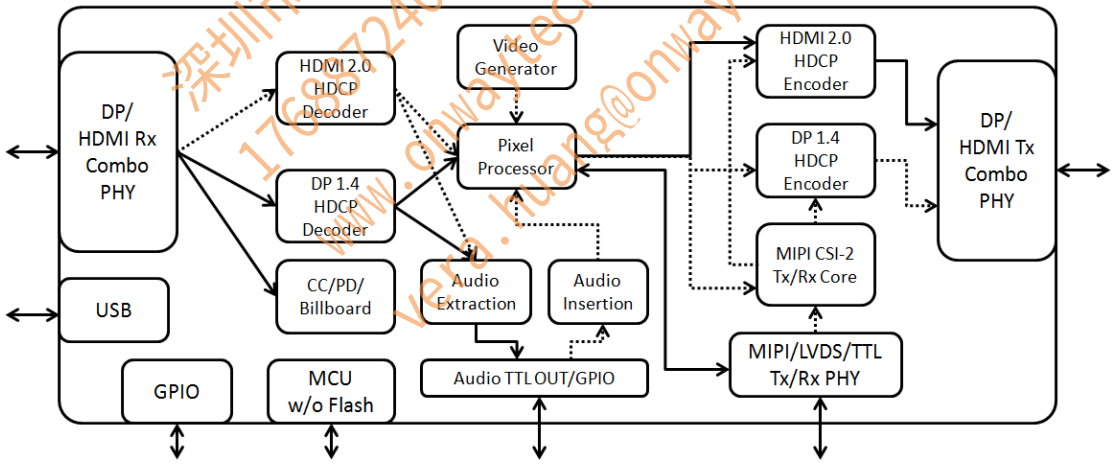


Figure 2. Type-C Alt-Mode In to HDMI Out with MIPI Out Application

1.3.2 HDMI In to Type-C Alt-Mode Out with MIPI Out Application

RxPort is configured as HDMI 2.0 Input. This mode is designed for HDMI 2.0 to SoC MIPI panel front-end interconnection. If required, the MIPI interface can also be set to LVDS/TTL for output (up to 4K60 420 timing). TxPort can be configured as DisplayPort or HDMI Output. When DisplayPort output is used for loop back, the application can also be

considered as HDMI to DisplayPort converter.

With internal Color Space Converter, De-Interlacer, HDMI 2.0 input timing can be converted to MIPI compatible output timing. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

Meanwhile, Audio extraction can be applicable if required.

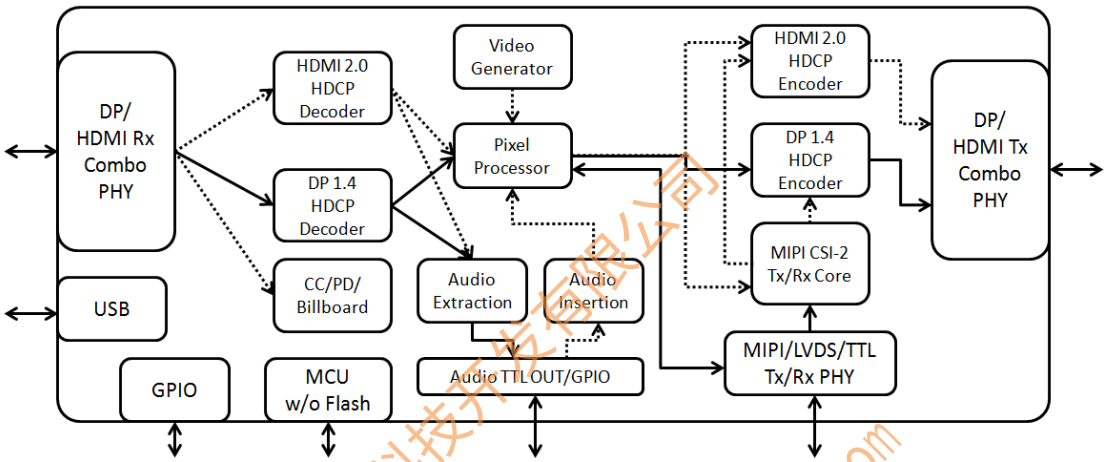


Figure 3. HDMI In to Type-C Alt-Mode Out with MIPI Out Application

1.3.3 MIPI In to HDMI/DisplayPort Out Application

TxPort is configured as HDMI 2.0 or DisplayPort Output. This mode is designed for SoC MIPI to HDMI 2.0/DisplayPort front-end interconnection. If required, the MIPI interface can also be set to LVDS/TTL for input (up to 4K60 420 timing).

With internal Color Space Converter, De-Interlacer, HDMI 2.0 output timing can be converted to any color space of RGB/YCbCr444/YCbCr422/YCbCr420.

Meanwhile, Audio insertion can be applicable if required.

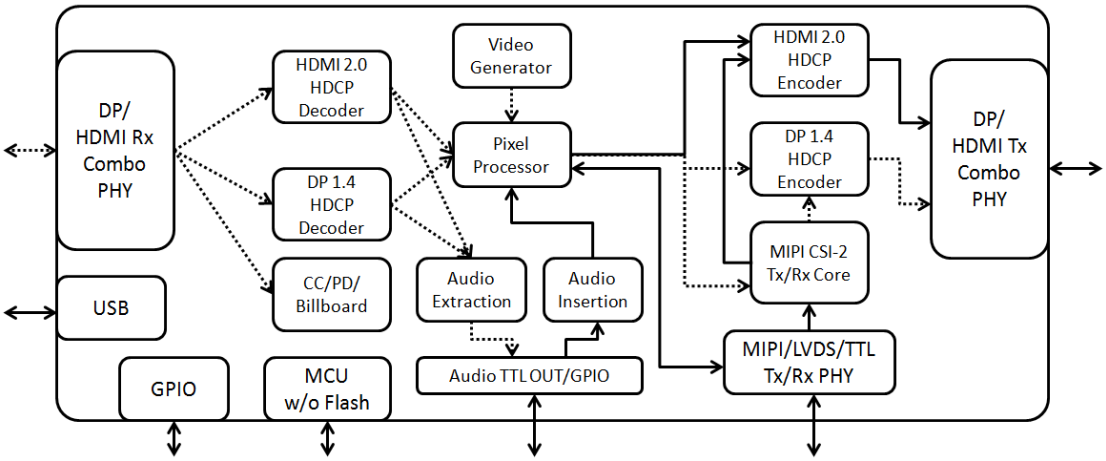


Figure 4. MIPI In to HDMI Out Application

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Output	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Output	I2S Data, 5/6 channels
AUD_D3	SDATA[3]	Output	I2S Data, 7/8 channels
AUD_D4	SPDIF	Output	SPDIF channel
AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Output	Fixed to 64Fs
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs

For HBR application, SPDIF is also capable of sending out with 4 pins.

Table 3. HBR Audio Extraction in SPDIF

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF[0]	Output	SPDIF Data[0], 1/2 channels
AUD_D1	SPDIF[1]	Output	SPDIF Data[1], 3/4 channels
AUD_D2	SPDIF[2]	Output	SPDIF Data[2], 5/6 channels
AUD_D3	SPDIF[3]	Output	SPDIF Data[3], 7/8 channels
AUD_D4	SPDIF	Output	SPDIF channel, 1/2 channels

2. Pin Description

2.1 Pin Diagram

QFN96 Pin definition is defined as below.

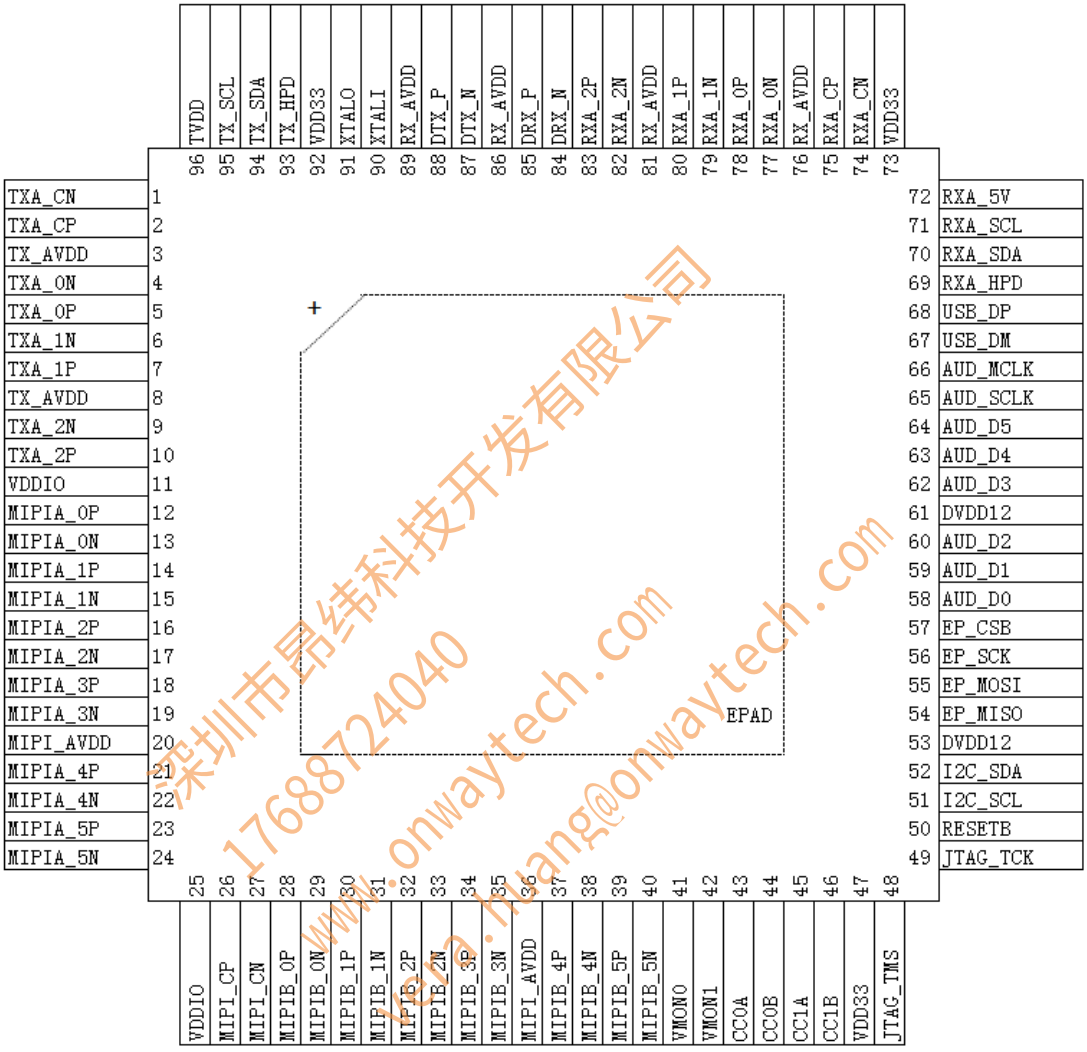


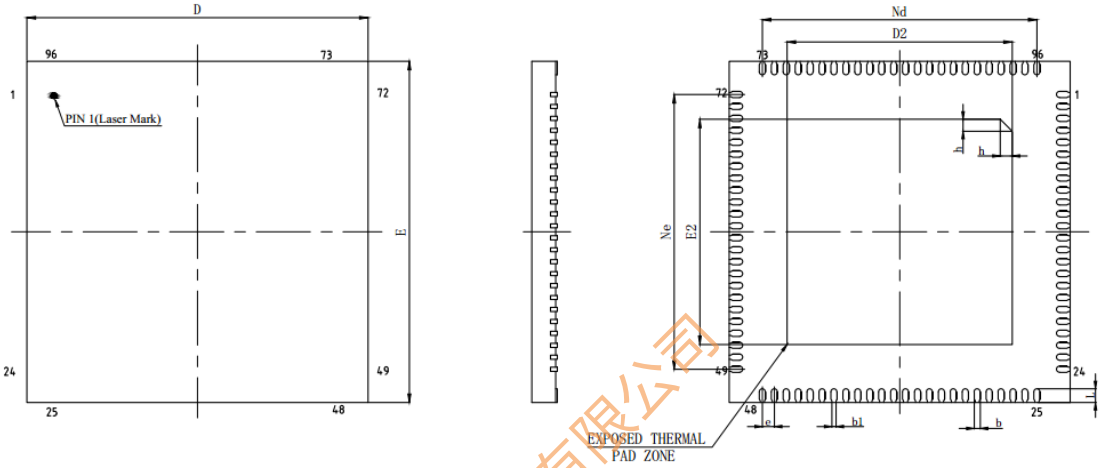
Figure 6. GSV6127X QFN96 Pin Diagram

2.2 QFN96 Pin Description

Table 9. QFN96 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI RX Pins/Type-C UFP/DisplayPort RX Pins			
RXA_5V	I	72	HDMI: RX 5V Detection PAD DP: RX DP Detection PAD

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.13	0.18	0.23
b1		0.12REF	
c	0.18	0.20	0.25
D	9.90	10.0	10.10
D2	6.50	6.60	6.70
e		0.35BSC	
Nd		8.05BSC	
E	9.90	10.0	10.10
E2	6.50	6.60	6.70
Ne		8.05BSC	
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 15. Package Dimensions (QFN96)

5. Ordering Guide

Table 18. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV6127X	-40°C to 85°C	QFN96	Tray