GSV1172

MIPI/LVDS to DisplayPort 1.2/ HDMI 1.4 Converter with Embedded MCU

May, 2024

Preliminary Product Specification

1. General Description

1.1 General Information

Gscoolink GSV1172 is a high-performance, low-power MIPI D-PHY CSI-2/DSI and LVDS VESA/JEIDA to DisplayPort 1.2/HDMI 1.4 converter. With Single Port MIPI interface, 4K30 RGB can be transmitted using single port MIPI interface. For LVDS VESA/JEIDA interface, 1080p60 RGB can be transmitted using single port LVDS interface. By integrating enhanced microcontroller, GSV1172 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Transmitter supports up to 21.6Gbps (HBR2, 4-lane), HDMI Transmitter supports up to 9Gbps (TMDS, 3G/3Lane). The superior architecture of GSV1172 provides economical smaller footprint solutions using QFN64, targeting for low power embedded applications.

HDCP 1.4 is implemented in GSV1172 for its HDMI/DisplayPort output. Color Space Conversion, 420-444/422 Conversion, De-Interlacer and Downscaler are supported for flexible video processing. Audio Insertion of HDMI/DisplayPort Tx is supported in GSV1172 for audio processing.

Within 8kV HBM tolerance, GSV1172's operation temperature range is -40 ºC to 85 ºC.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 1.4 bandwidth, such as 4K@30Hz, 1080P@60Hz, 480i@60Hz.

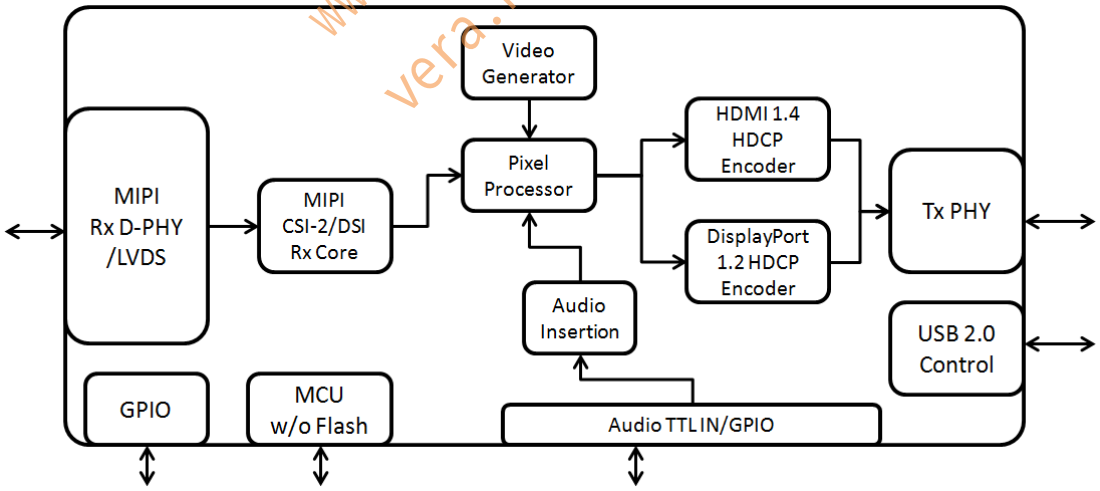


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 HDMI Transmitter Features

- Compliant with HDMI 1.4b
- Compliant with HDCP 1.4
- Data rate up to 9Gbps (TMDS 3Gbps/3 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS input/output
- Support Color Space Converter in TMDS mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

1.2.2 DisplayPort Transmitter

- Compliant with VESA DisplayPort 1.2a
- Compliant with HDCP 1.4
- Support HBR2, HBR and RBR (5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Insertion
- Support Spread Spectrum Clock (SSC)
- 3D format support of stacked frame, side-by-side, top-to-bottom

1.2.3 MIPI CSI-2/DSI-2 Receiver

- Support MIPI CSI-2 v3.0 version receiving using D-PHY interface
- Support MIPI DSI-2 v2.0 version receiving using D-PHY interface
- Support 2.5G bps 1/2/3/4-lane MIPI D-PHY Input
- CSI-2/DSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

1.2.4 Single-Port LVDS Receiver

- Compatible with VESA and JEIDA standards
  - Single -Port LVDS Receiver
  - Data rate up to 1.5Gbps per lane

1.2.5 Pixel Processor

- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with fixed horizontal and vertical 2 ratio for 4K to 2K conversion
- Deinterlacer for interlaced timing

1.2.6 Audio Input

- I2S and SPDIF Audio Insertion to HDMI Tx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Insertion

1.2.7 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 MIPI/LVDS In to HDMI Out Application

TxPort is configured as HDMI 1.4 Output. This mode is designed for SoC MIPI/LVDS to HDMI 1.4 front-end interconnection. SoC can stream out a fixed timing via MIPI, and stream I2S audio to generate HDMI output by GSV1172.

With internal Color Space Converter, De-Interlacer, HDMI 1.4 output timing can be converted to any color space of RGB/YCbCr444/YCbCr422/YCbCr420. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

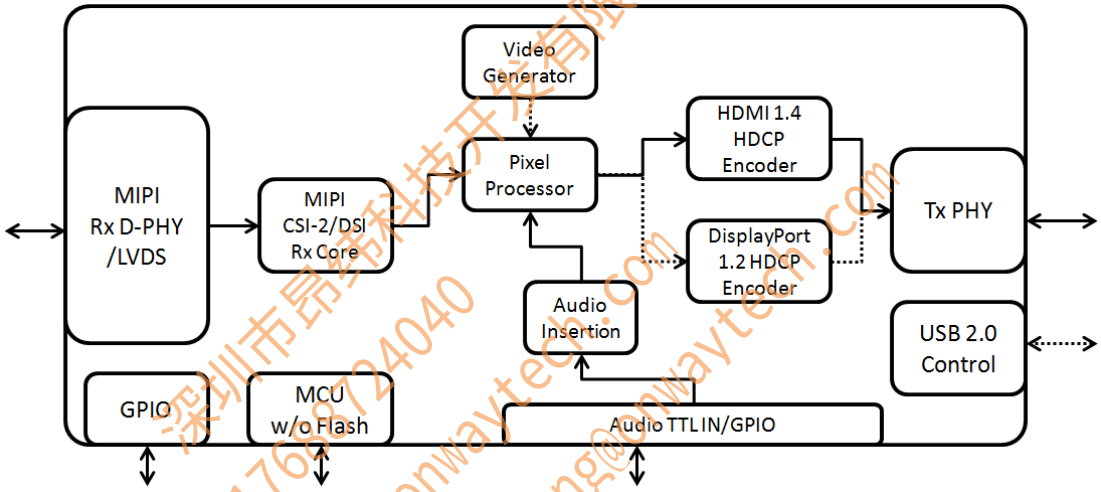


Figure 2. MIPI In to HDMI Out Application

1.3.2 MIPI/LVDS In to DisplayPort Out Application

TxPort is configured as DisplayPort 1.2 Output. This mode is designed for SoC MIPI/LVDS to DisplayPort 1.2 front-end interconnection. SoC can stream out a fixed timing via MIPI, and stream I2S audio to generate DisplayPort output by GSV1172.

With internal Color Space Converter, De-Interlacer, DisplayPort 1.2 output timing can be converted to any color space of RGB/YCbCr444/YCbCr422/YCbCr420. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

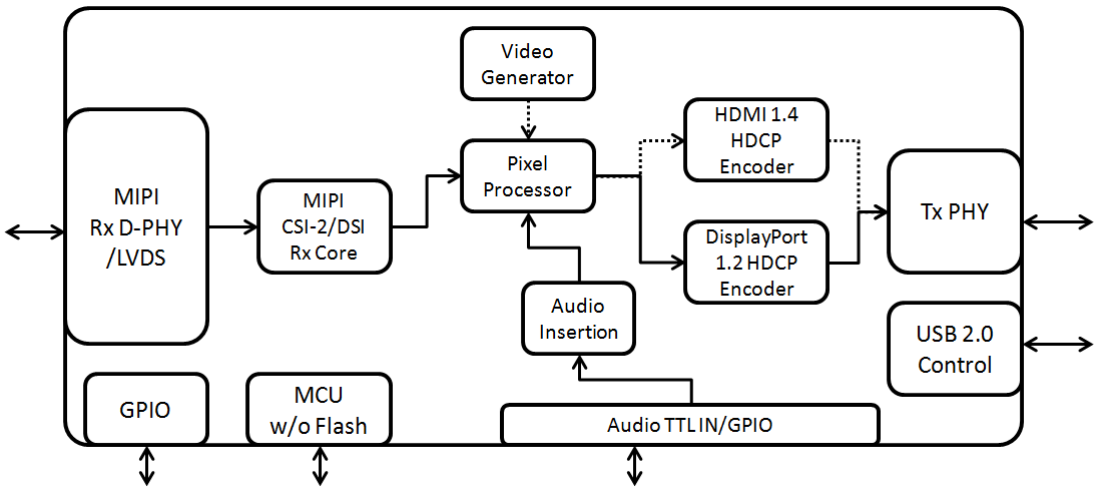


Figure 3. MIPI In to DisplayPort Out Application

1.4 Audio Bus Input Configuration

When Audio Bus is set to Input, either I2S or SPDIF can be selected. It should be noted that external MCLK is required in I2S audio insertion mode.

For SPDIF input, GSV1172 can detect Sampling Frequency and automatically update it in Channel Status with GSV software. For I2S input, software designer needs to indicate the input sampling frequency in software. General application modes are listed below.

Table 2. Stereo I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

Table 3. SPDIF Input

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF	Input	SPDIF channel

Table 4. 6-Channel I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Input	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Input	I2S Data, 5/6 channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)

2. Pin Description

2.1 Pin Diagram

QFN64 Pin definition is defined as below.

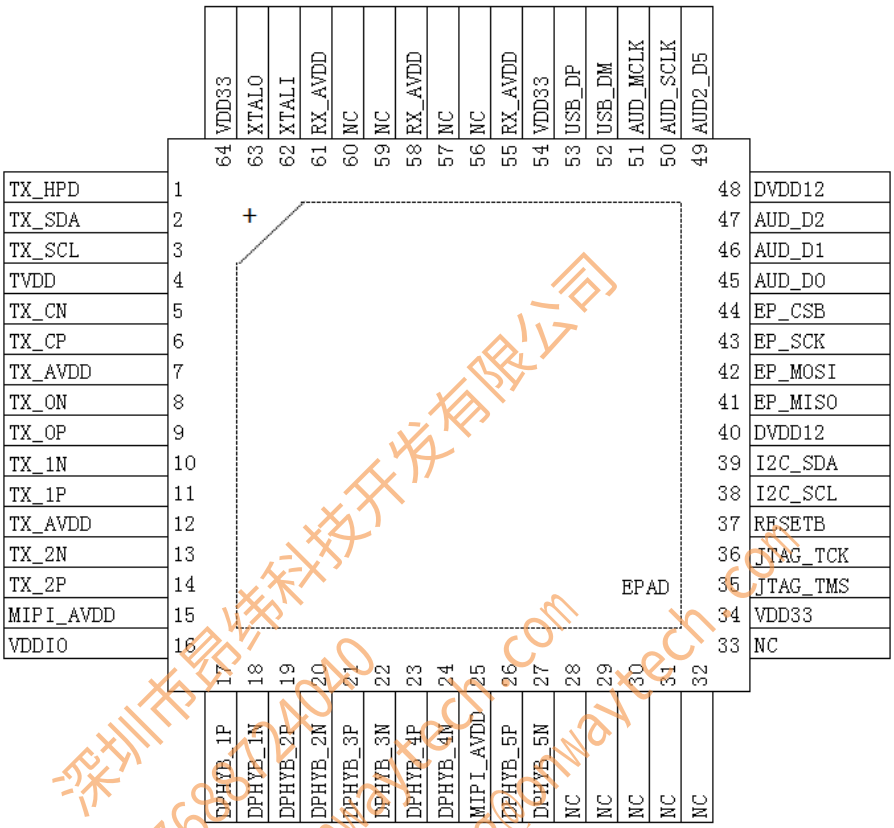


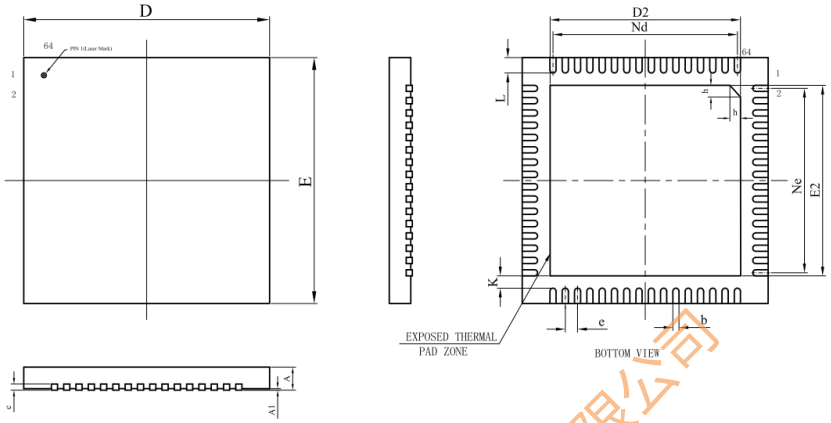
Figure 4. GSV1172 QFN64 Pin Diagram

2.2 QFN64 Pin Description

Table 5. QFN64 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI/DisplayPort TX Pins			
TX_SDA	I/O	2	HDMI: TXA DDC SDA PAD DP: TXA AUX_P PAD
TX_SCL	I/O	3	HDMI: TXA DDC SCL PAD DP: TXA AUX_N PAD
TX_HPD	I	1	HDMI: TXA HPD PAD DP: TXA HPD PAD
TX_CN	O	5	HDMI: TXA Negative TMDS clock differential output DP: TXA Negative Main-Link differential data output [3]

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	7.90	8.00	8.10
D2	6.10	6.20	6.30
e	0.40BSC		
Nd	6.00BSC		
E	7.90	8.00	8.10
E2	6.10	6.20	6.30
Ne	6.00BSC		
L	0.45	0.50	0.55
K	0.20	—	—
h	0.30	0.35	0.40
载体尺寸 (mil)	258*258		

Figure 8. Package Dimensions (QFN64)

5. Ordering Guide

Table 10. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV1172	-40°C to 85°C	QFN64	Tray