GSV1173

MIPI/LVDS to Embedded DisplayPort(eDP) 1.2 Converter with Embedded MCU

May, 2024

Preliminary Product Specification

1. General Description

1.1 General Information

Gscoolink GSV1173 is a high-performance, low-power MIPI D-PHY CSI-2/DSI and LVDS VESA/JEIDA to Embedded DisplayPort(eDP) 1.2 converter. With Single Port MIPI interface, 4K60 422 can be transmitted using single port MIPI interface. For LVDS VESA/JEIDA interface, 1080p60 RGB can be transmitted using single port LVDS interface. By integrating enhanced microcontroller, GSV1173 has created a cost-effective solution that provides time-to-market advantages. The eDP Transmitter supports up to 21.6Gbps (HBR2, 4-lane). The superior architecture of GSV1173 provides economical smaller footprint solutions using QFN64, targeting for low power embedded applications.

Color Space Conversion, 420-444/422 Conversion, De-Interlacer and Downscaler are supported for flexible video processing.

Within 4kV HBM tolerance, GSV1173's operation temperature range is -40 ºC to 85 ºC.

An internal Video Generator can be used to generate any uncompressed video timing defined in DisplayPort HBR2 bandwidth, such as 4K@30Hz, 1080P@60Hz, 480i@60Hz.

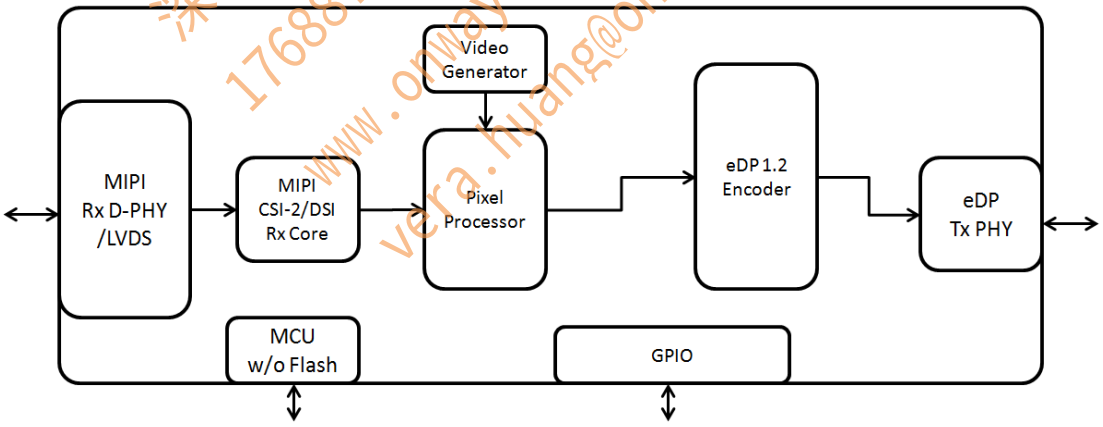


Figure 1. Top Diagram

1.2 Features

1.2.1 Embedded DisplayPort Transmitter

- Compliant with VESA Embedded DisplayPort 1.2a

- Support HBR2, HBR and RBR (5.4/2.7/1.62 Gbps)
- Support 2.16/2.43/3.24/4.32 Gbps
- Support Backlight Control and MCCS over AUX
- Support ASSR
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Spread Spectrum Clock (SSC)
- 3D format support of stacked frame, side-by-side, top-to-bottom

1.2.2 MIPI CSI-2/DSI-2 Receiver

- Support MIPI CSI-2 v3.0 version receiving using D-PHY interface
- Support MIPI DSI-2 v2.0 version receiving using D-PHY interface
- Support 2.5G bps 1/2/3/4-lane MIPI D-PHY Input
- CSI-2/DSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

1.2.3 Single-Port LVDS Receiver

- Compatible with VESA and JEIDA standards
  - Single -Port LVDS Receiver
  - Data rate up to 1.5Gbps per lane

1.2.4 Pixel Processor

- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with fixed horizontal and vertical 2 ratio for 4K to 2K conversion
- Deinterlacer for interlaced timing

1.2.5 System Features

- Optional External MCU (via I2C)/ Internal MCU mode

- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 MIPI/LVDS In to eDP Out Application

TxPort is configured as Embedded DisplayPort 1.2 Output. This mode is designed for SoC MIPI/LVDS to eDP Tcon front-end interconnection. SoC can stream out a fixed timing via MIPI to generate eDP output by GSV1172.

With internal Color Space Converter, De-Interlacer, DisplayPort 1.2 output timing can be converted to any color space of RGB/YCbCr444/YCbCr422/YCbCr420. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

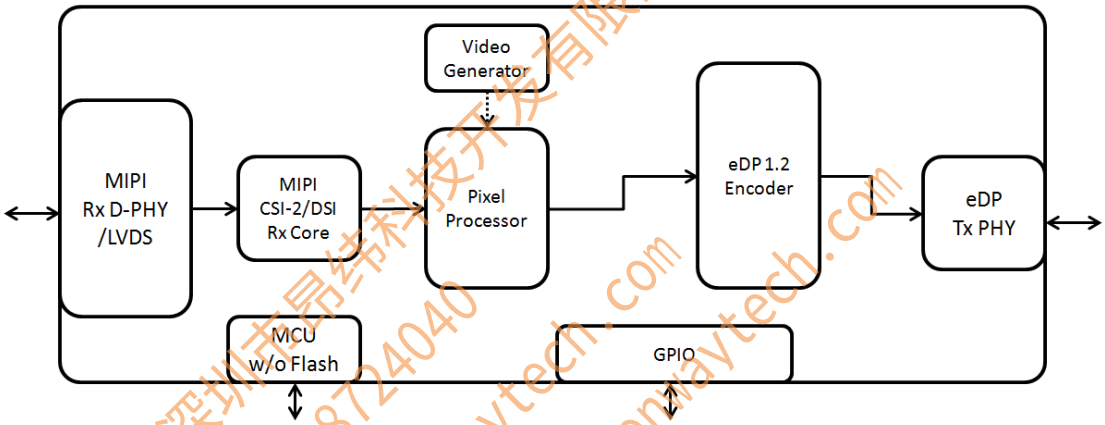


Figure 2. MIPI In to eDP Out Application

2. Pin Description

2.1 Pin Diagram

QFN64 Pin definition is defined as below.

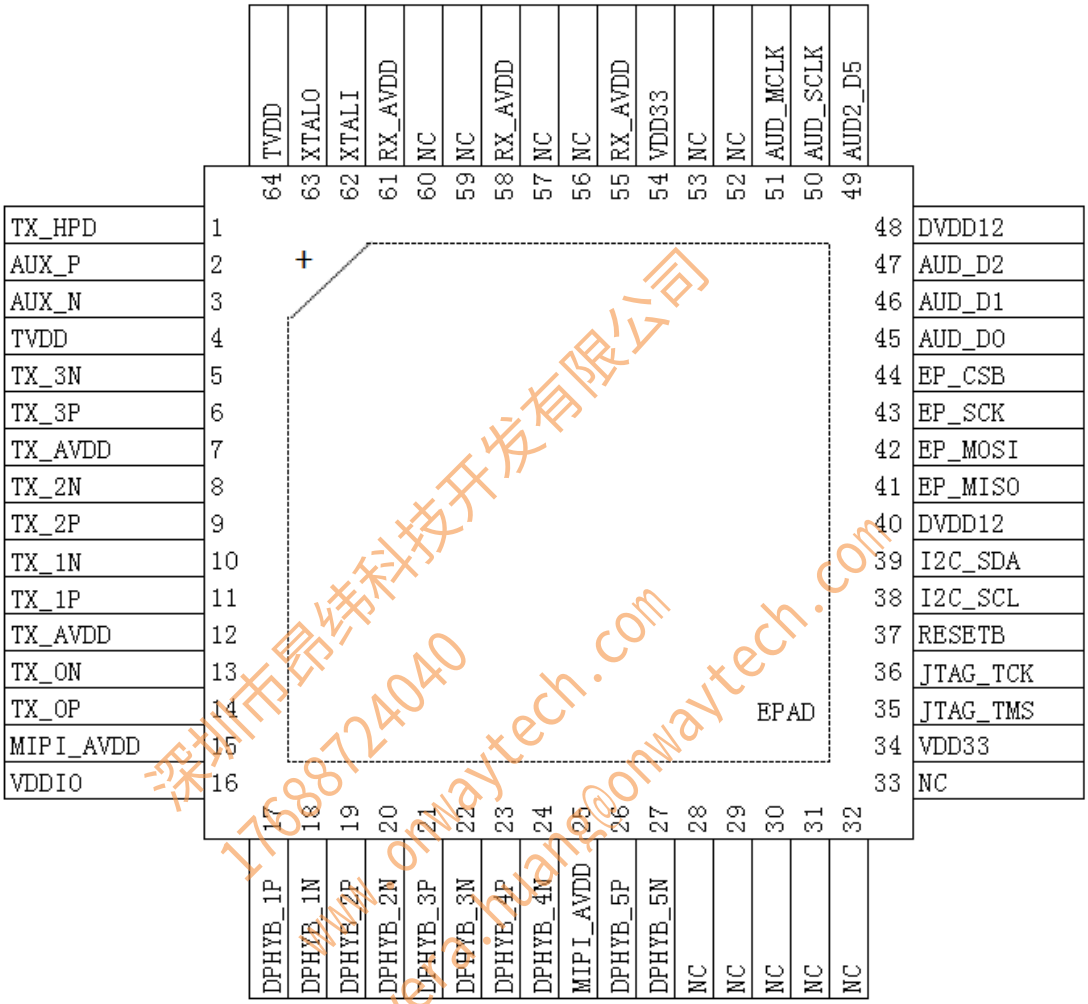


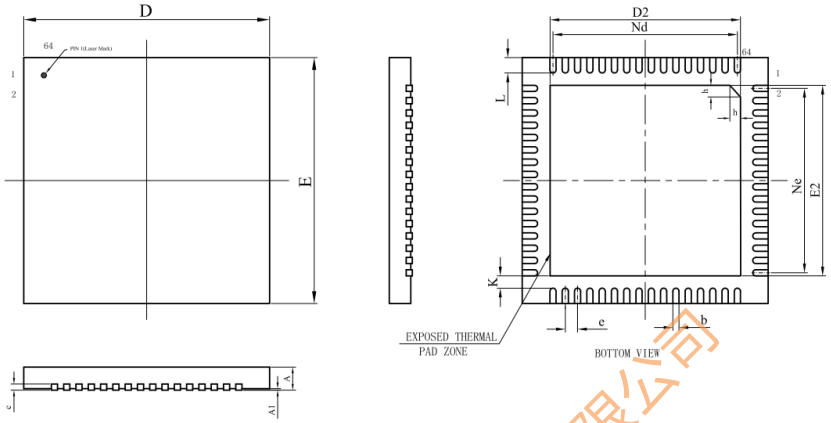
Figure 3. GSV1173 QFN64 Pin Diagram

2.2 QFN64 Pin Description

Table 1. QFN64 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI TX Pins/ Type-C DFP/DisplayPort TX Pins			
AUX_P	I/O	2	DP: TXA AUX_P PAD
AUX_N	I/O	3	DP: TXA AUX_N PAD
TX_HPD	I	1	DP: TXA HPD PAD
TX_3N	O	5	DP: TXA Negative Main-Link differential data output [3]

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	7.90	8.00	8.10
D2	6.10	6.20	6.30
e	0.40BSC		
Nd	6.00BSC		
E	7.90	8.00	8.10
E2	6.10	6.20	6.30
Ne	6.00BSC		
L	0.45	0.50	0.55
K	0.20	—	—
h	0.30	0.35	0.40
载体尺寸 (mil)	258*258		

Figure 7. Package Dimensions (QFN64)

5. Ordering Guide

Table 4. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV1173	-40°C to 85°C	QFN64	Tray